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DESIGN AND ANALYSIS OF AN ELECTRONICALLY STEERABLE MICROSTRIP PATCH AND A NOVEL COPLANAR WAVEGUIDE (CPW) FED SLOT ANTENNA ARRAY

by

Hamad Aldossary

Bachelor of Engineering
University of South Carolina, 2011

Submitted in Partial Fulfillment of the Requirements

For the Degree of Master of Science in

Electrical Engineering

College of Engineering and Computing

University of South Carolina

2013

Accepted by:

Dr. Mohammod Ali, Major Professor

Dr. Grigory Simin, Committee Member

Dr. Lacy Ford, Vice Provost and Dean of Graduate Studies

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DEDICATION

This thesis is dedicated to my wife Stephanie; her love, patience, support and understanding have lightened up my spirit to finish this study and this thesis.

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ACKNOWLEDGEMENTS

All praises belong to Allah Almighty. By His will, I got a lot of help, support and encouragement from individuals which enabled me finish my study in the Department of Electrical Engineering at the University of South Carolina at Columbia.

I would like to express my sincere gratitude to my advisor Dr. Mohammod Ali for the continuous support of my Master of Science study and research, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. I could not have imagined having a better advisor and mentor for my Master of Science study.

Last but not the least; I would like to thank my family and my family in law for supporting me throughout my life.

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ABSTRACT

Conformal Phased Array Antennas (CPAAs) are very attractive for their high gain, low profile, and beam scanning ability while being conformal to their mounting surface. Among them are microstrip patch phased arrays and wideband slot phased arrays which are of particular significance.

In this work, first the study, design, and implementation of a conformal microstrip patch phased array is presented which consists of a high gain beam scanning array implemented using microstrip delay lines controlled using GaAs SPDT switches. Then the study and design of a wideband Coplanar Waveguide (CPW)-fed slot phased array antenna is presented. In both cases the array beam scanning properties are elucidated by incorporating the measured delay line scattering parameters inside Ansys Designer simulation models and then computing and presenting their full-wave radiation characteristics.

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CHAPTER 1

INTRODUCTION TO PHASED ARRAY ANTENNAS

Phased array antennas are in great demand for commercial as well as military applications because of their advantages of higher gain and beam steering capability without any mechanical movement of the antenna platform. Electronically steering the beam of the array would require that the elements of the array are excited at different phases. This is generally achieved using electronic phase shifters consisting of transmission lines controlled using switches.

While a phased array can be designed and developed at any frequency we focus on the 2 GHz frequency band because of its proximity to many practical applications, e.g. mobile telephone, IEEE 802.11 WLAN, GPS (1.575 GHz), and UMTS (Universal Mobile Telecommunication Systems). The thesis begins with the basic introduction of microstrip patch antennas then standard array theory is introduced in brief after which we delve into the discussions of phased array antennas. First, a microstrip patch phased array

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design is presented then the analysis of a wideband CPW-fed slot phased array is presented.

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CHAPTER 2

MICROSTRIP PATCH ANTENNA

2.1 Introduction to Microstrip Patch Antenna

Microstrip patch antennas are one of the simplest antennas to fabricate. They are low profile and inexpensive to fabricate. Patch antenna is conformal to planar and non-planar surfaces[1]. Microstrip patch antenna consists of a radiating element on one side and a dielectric on the other, the bottom of the dielectric contains the ground, as shown in Figure 2.1[2].

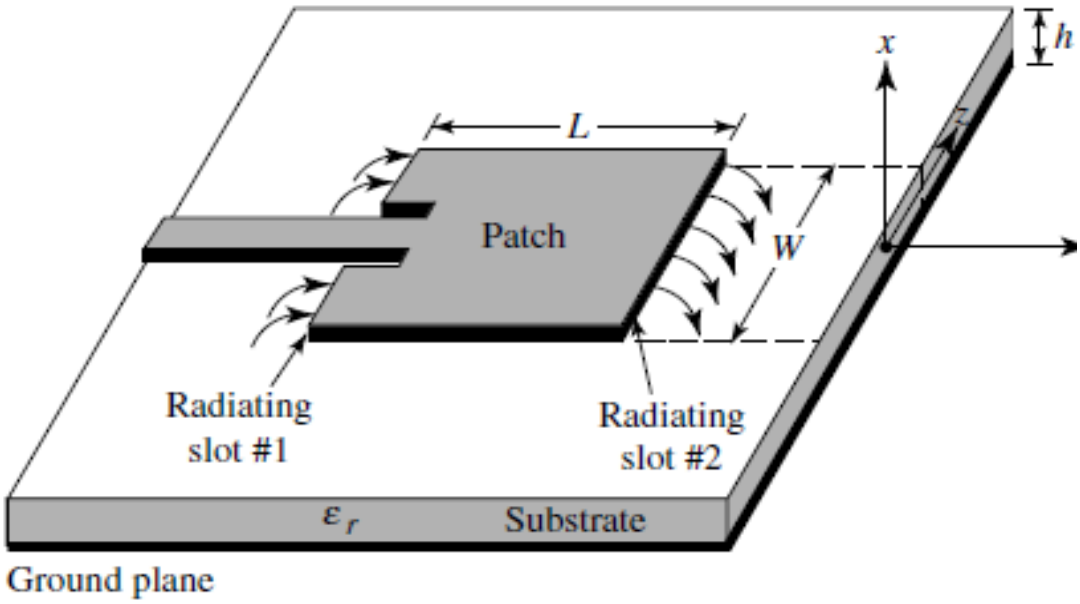

Figure 2.1 Microstrip antenna[3].

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Microstrip patch antenna come in many shapes such as square, rectangular, circular, triangular, and elliptical or some other common shape as shown in Figure 2.2[1].

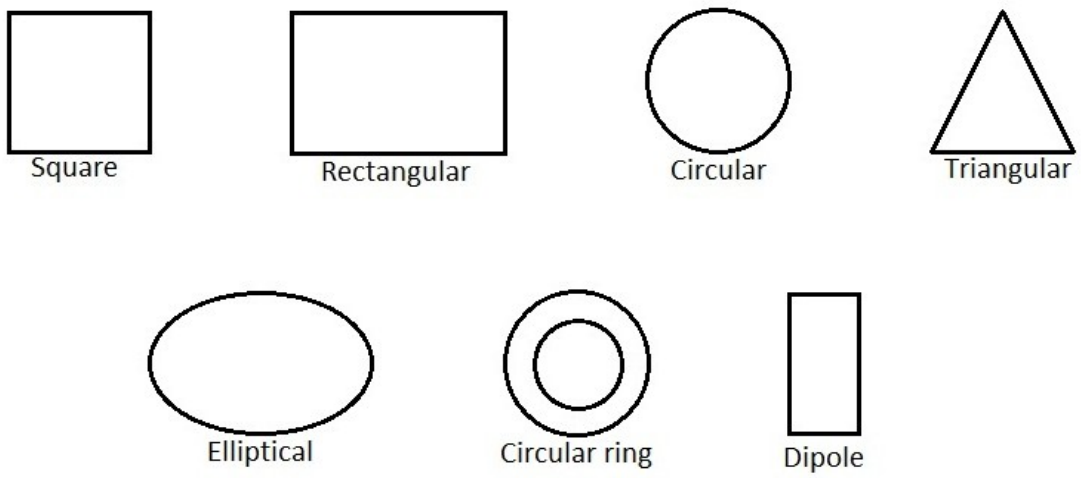

Figure 2.2 Representative shapes of microstrip patch elements[3].

Patch antenna radiates due to the fields coming out from radiating slot 1 and going into radiating slot 2 as shown in Figure 2.1[1].

2.2 Feeding Methods

Microstrip patch antennas can be fed by different methods. Generally, the methods could be categorized as contact method and non-contact method. In the contact method, the power is fed directly to the patch. In the non-contact method, the power is transferred through coupling

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between the microstrip line and the patch. The four most popular feed techniques used are the microstrip line, coaxial probe, aperture coupling and proximity coupling[4].

The microstrip type feeding features a conducting strip that is connected directly to the edge of the microstrip patch as shown in Figure 2.3.

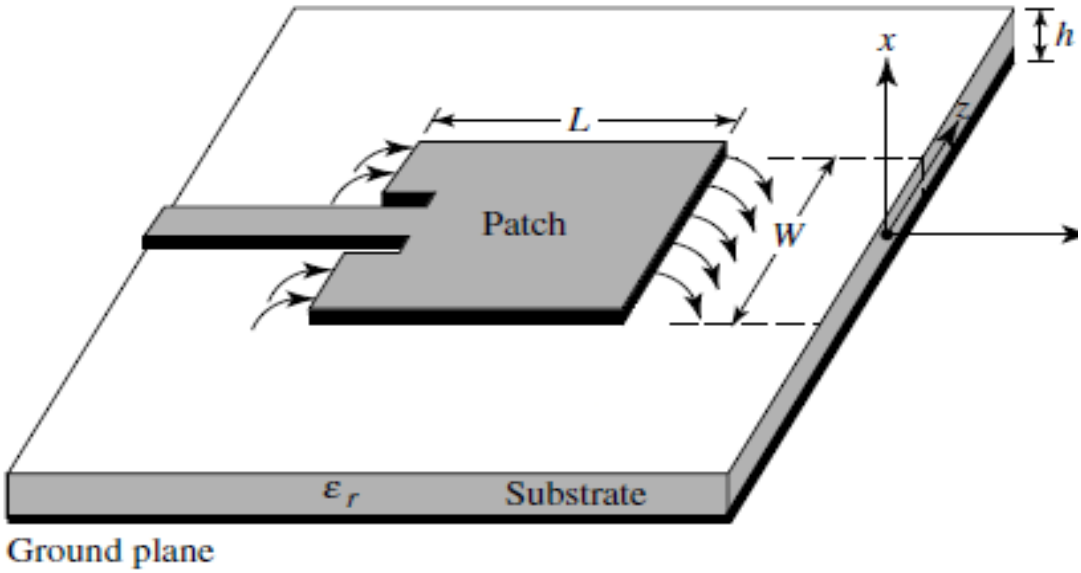

Figure 2.3 Microstrip line feed[3].

The microstrip feed line is easy to fabricate, and simple to match by controlling the inset position. The purpose of the inset in the patch is to match the impedance of the feed line to the patch, and it can be achieved by choosing the proper length of the inset[4].

The Coaxial feed is a very common technique used for feeding microstrip patches antennas. As seen from Figure

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2.4, the inner conductor of the coaxial connector is attached to the radiating patch, while the outer conductor is connected to the ground plane.

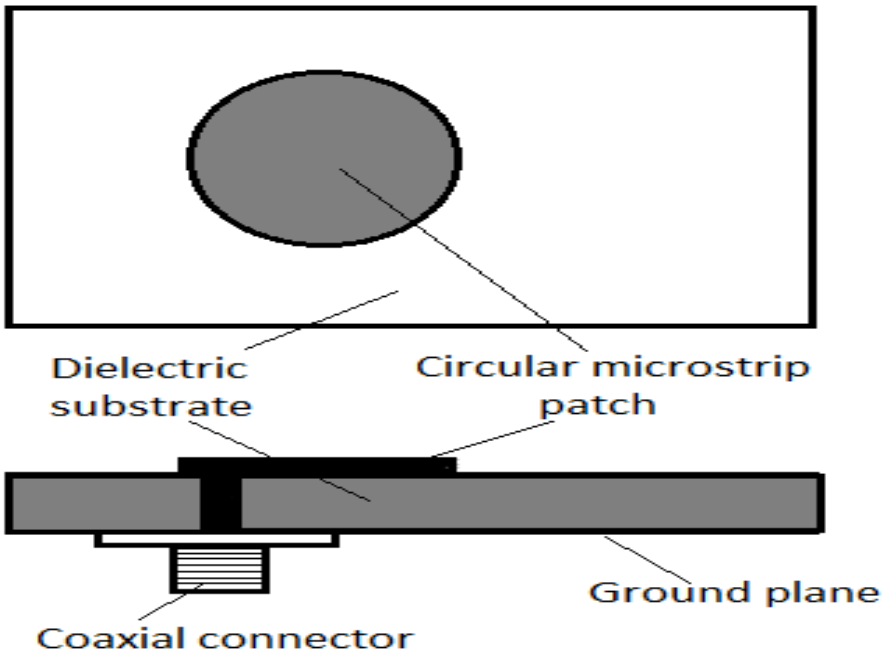

Figure 2.4 Probe feed[3].

The advantage of using this feeding technique is that the feed can be positioned at the correct location to match the impedance of the input. It is easy to fabricate and has low spurious radiation. However, it provides a narrow bandwidth and is difficult to model, a hole has to be drilled through the substrate, especially thick substrates[5].

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Aperture coupling feed is difficult to fabricate and it has a narrow bandwidth. Yet, it has a moderate spurious radiation. Aperture coupling consists of two substrates separated by a ground plane. On the lower substrate there is a microstrip line that couples its energy to the patch on the upper substrate through a slot on the ground plane, as shown in the Figure 2.5.

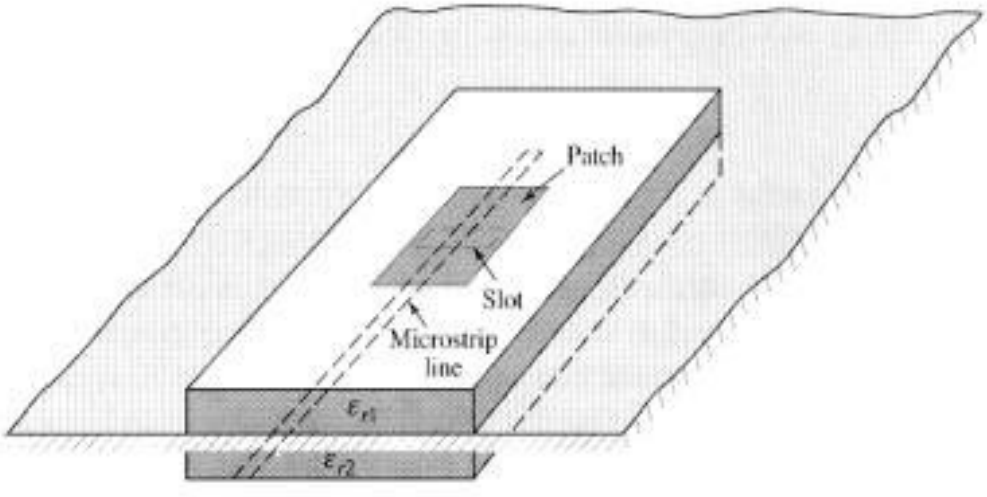

Figure 2.5 Aperture-coupled feed[3].

On all of the feeding techniques, the following feeding method by far has the largest bandwidth (as high as 13%). It consists of two substrates, the top of the lower substrate has the feed line and the radiating element is on the top of the higher substrate [6]-[37]. This feeding method is called Proximity-coupled feed, as shown in Figure 2.6.

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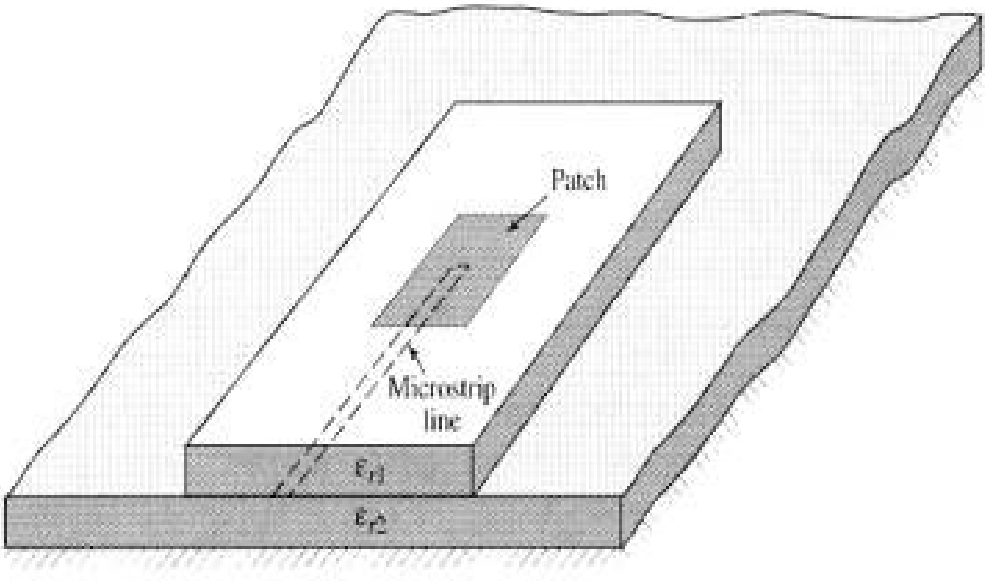

Figure 2.6 Proximity-coupled feed[3].

The proximity-coupled feed is somewhat easy to model, yet it is hard to fabricate. It has low spurious radiation. The feed line length and the width to line ratio of the radiating element are used to attain optimum matching[6].

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CHAPTER 3

LINEAR ARRAY

3.1 Introduction

It is well known that high directivity can be achieved by forming an antenna array consisting of individual radiating elements, antennas, in a specific electrical and geometrical configuration[7]. This occurs because of the vector addition of the total fields radiated by each element. Designing a very directive pattern requires the fields of the elements to interfere constructively in the desired directions and interfere destructively in the remaining space[8].

3.2 Two-Element Array

Let us assume that two infinitesimal dipoles are positioned horizontally on the z-axis as shown in **Figure 3.1.**

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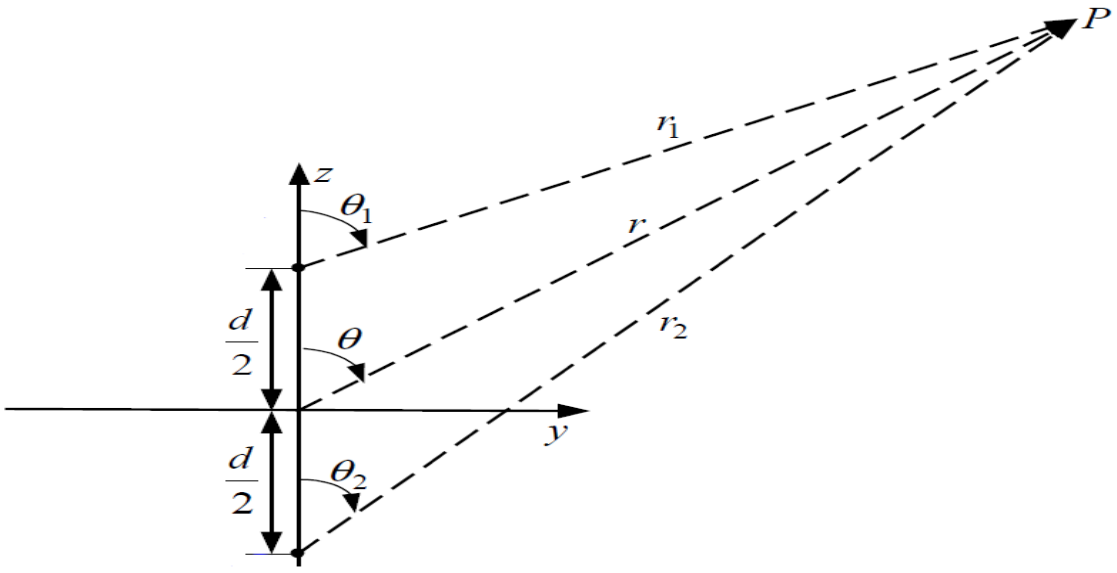

Figure 3.1 Geometry of a two element array consisting of two infinitesimal dipoles[3].

Assuming no coupling between the two elements, the total radiated field is equal to the sum of the fields radiated by the two elements and is given by

$$E_t = E_1 + E_2 = \hat{a}_\theta j\eta \frac{kI_0 l}{4\pi}\{\frac{e^{-j\left[kr_1-\left(\frac{\beta}{2}\right)\right]}}{r_1}cos\theta_1 + \frac{e^{-j\left[kr_2+\left(\frac{\beta}{2}\right)\right]}}{r_2}cos\theta_2\} \qquad (3.1)$$

where β is the difference in phase excitation between the radiating elements. The excitation magnitude of the radiating elements is identical[7]. The far field can be approximated by redrawing **Figure 3.1,** as shown in Figure 3.2.

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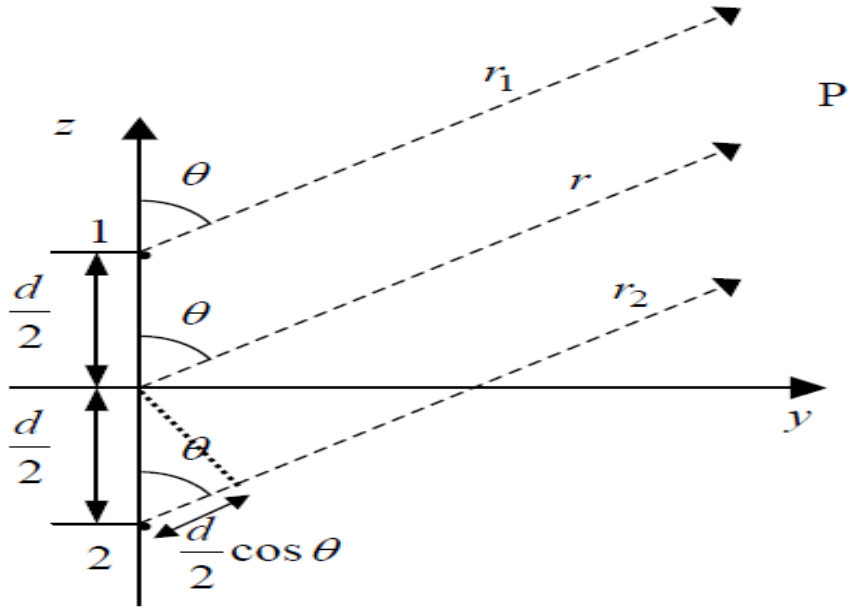

Figure 3.2 Far field observation of the two-element array[3]

Observing **Figure 3.2** would set the following assumptions

$$\theta_1 \cong \theta_2 \cong \theta$$

$$\left.\begin{aligned} r_1 &\cong r - \frac{d}{2}cos\theta \\ r_2 &\cong r + \frac{d}{2}cos\theta \end{aligned}\right\} for\ phase\ variations$$

$$r_1 \cong r_2 \cong r\ for\ amplitude\ variations$$

These approximations would reduce Equation (3.1) to

$$E_t = \hat{a}_\theta j\eta \frac{kI_0 l e^{-jkr}}{4\pi r} cos\theta [e^{+j(k\ d\ cos\theta+\beta)/2} + e^{-j(k\ d\ cos\theta+\beta)/2}] \quad (3.2)$$

After using Euler's identity

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$$E_t = \hat{a}_\theta j\eta \frac{kI_0 l e^{-jkr}}{4\pi r} cos\theta \{2\cos[\frac{1}{2}(k\, d \cos\theta + \beta)]\} \qquad (3.3)$$

The above relation is generally referred to as pattern multiplication which shows that the total field of the array is equal to the product of the field due to the single element positioned at origin and the a factor called the array factor. The factor inside the curly bracket is the array factor here.

3.3 N-Element Uniform Linear Array

After introducing the array concept consisting of two elements, we could generalize the concept to include an N-element uniform linear array. A uniform array is an array that consists of identical elements with the same excitation amplitude[7].

3.3.1 N-Element Array Factor

Observing the geometry of **Figure 3.3,** we will assume that all the radiating elements have the same excitation amplitude but each succeeding element has a progressive phase difference β compared to the previous element[38]-[54].

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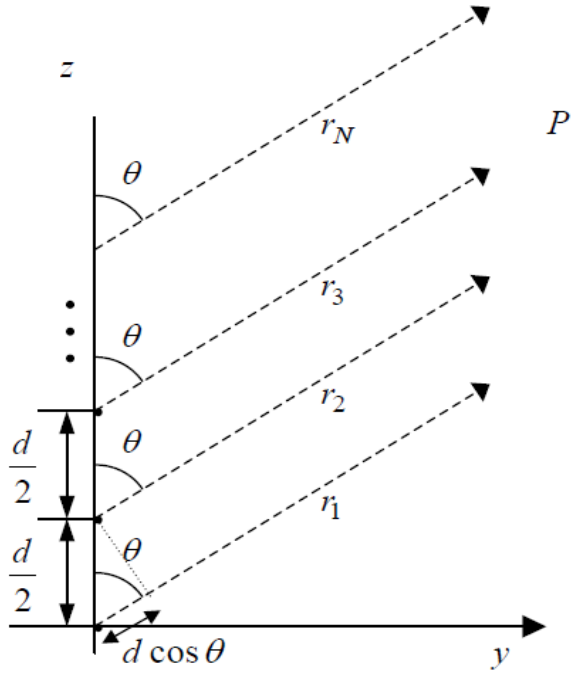

Figure 3.3 Far field geometry of N-element array[3].

Considering the elements to be point sources, the array factor can be obtained[7]. The array factor of an N-element linear array with uniform amplitude and spacing is given by,

$$AF = \sum_{n=1}^{N} e^{j(n-1)\psi} \tag{3.4}$$

$$\psi = kd\cos\theta + \beta \tag{3.5}$$

Therefore, by varying β the array factor of the array can be controlled.

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3.3.2 Broadside Array

Some applications require the array to have the maximum radiation normal to the axis of the array, called Broadside Array. The maximum of the array factor and the single element have to be directed toward $\theta_0=90^\circ$. This can be accomplished with the array factor by choosing the proper separation and excitation between each radiating element[7]. The broadside condition occurs when $\theta_0=90^\circ$,

$$\psi = kd\cos\theta + \beta|_{\theta=90^\circ} = \beta = 0 \qquad (3.6)$$

3.3.3 End-Fire Array

We could design the maximum radiation to occur along the axis of the array (end-fire) by choosing $\theta_0=0^\circ$ or $\theta_0=180^\circ$. Not only that but also we could design the maximum radiation to occur either on $\theta_0=0^\circ$ or $\theta_0=180^\circ$[7].

3.3.4 Phased (Scanning) Array

Directing the major radiation of an array in a specific angular direction can be accomplished by controlling the progressive phase difference between the radiating elements. Assuming that the maximum radiation of

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the array can be oriented at any angle θ_0 between 0˚ and 180˚, the required phase excitation β between each radiating element has to be computed using the following formula

$$\beta = -k\, d\, cos\theta_0 \qquad (3.7)$$

We could see from the above equation that controlling the progressive phase difference between each radiating element, the maximum radiation can be formed and steered in any desired direction to form a phased array[7].

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CHAPTER 4

PROPOSED PHASED ARRAY RECTANGULAR MICROSTRIP PATCH ANTENNA

4.1 Single Element Microstrip Patch Antenna

A resonance frequency of 2 GHz was selected for the baseline microstrip patch design. The dielectric substrate used was Duroid 5880 (relative permittivity $\varepsilon_r = 2.2$ and loss tangent $\delta = 0.0009$). The substrate thickness (h) was 1.55 mm. Table 4.1 below shows the basic design parameters of the patch under consideration.

Table 4.1 The basic parameters of the single element microstrip patch antenna.

Type of the antenna	Rectangular patch antenna
Dielectric constant (ε_r)	2.2
Resonant frequency	2 GHz
Substrate thickness (h)	1.55 mm
Feeding method	Inset feeding
Polarization	Linear

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Equation (4.1) is introduced to determine the optimum width (w) of a microstrip patch antenna as Balanis introduced in his Antenna Theory book[7],

$$W = \frac{c}{2f_r}\sqrt{\frac{2}{\varepsilon_r + 1}} \tag{4.1}$$

where c is the velocity of light. Substituting the following values, c = 3x10^8 m/s, f_r = 2 GHz and ε_r = 2.2; we find W = 59.2 mm. From [7] the effective dielectric constant ε_{reff} is calculated using Equation (4.2),

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12h/W}} \tag{4.2}$$

After calculating the value of ε_{reff}, we use equations (4.3a) and (4.3b) to determine the physical length of the patch,

$$\Delta L = h(0.412)\frac{(\varepsilon_{reff} + 0.3)(\frac{W}{h} + 0.264)}{(\varepsilon_{reff} - 0.258)(\frac{W}{h} + 0.8)} \tag{4.3a}$$

$$L = \frac{1}{2f_r\sqrt{\varepsilon_{reff}}\sqrt{\mu_0\varepsilon_0}} - 2\Delta L \tag{4.3b}$$

The calculated length of the patch is L = 54.6 mm. The feeding technique used was an inset feeding. The location of the inset feed point with respect to the patch can be calculated after finding the patch conductance and

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considering the feed impedance to be 50Ω. From [7], equations (4.4a) and (4.4b) for calculating the patch conductance is introduced,

$$G_1 = \frac{I_1}{120\pi^2} \tag{4.4a}$$

Where

$$I_1 = \int_0^{\pi} \left[\frac{\sin\left(\frac{k_0 W}{2}\cos\theta\right)}{\cos\theta} \right]^2 sin^3\theta \, d\theta \tag{4.4b}$$

$$= -2 + \cos(X) + XS_i(X) + \frac{sin(X)}{X}$$

and $X = k_0 W$. The conductance G_1 was found to be 0.001568 S. Assuming that the mutual conductance between the radiating edges of the patch is small, and ignoring its contribution to the overall patch conductance, the inset is given by[7],

$$y_0 = \frac{L \cos^{-1}(\sqrt{2Z_0 G_1})}{\pi} \tag{4.5}$$

where Z_0 is the characteristic impedance of the feed line. The inset length was found to be 19.5 mm. **Figure 4.1** shows the patch geometry and dimensions.

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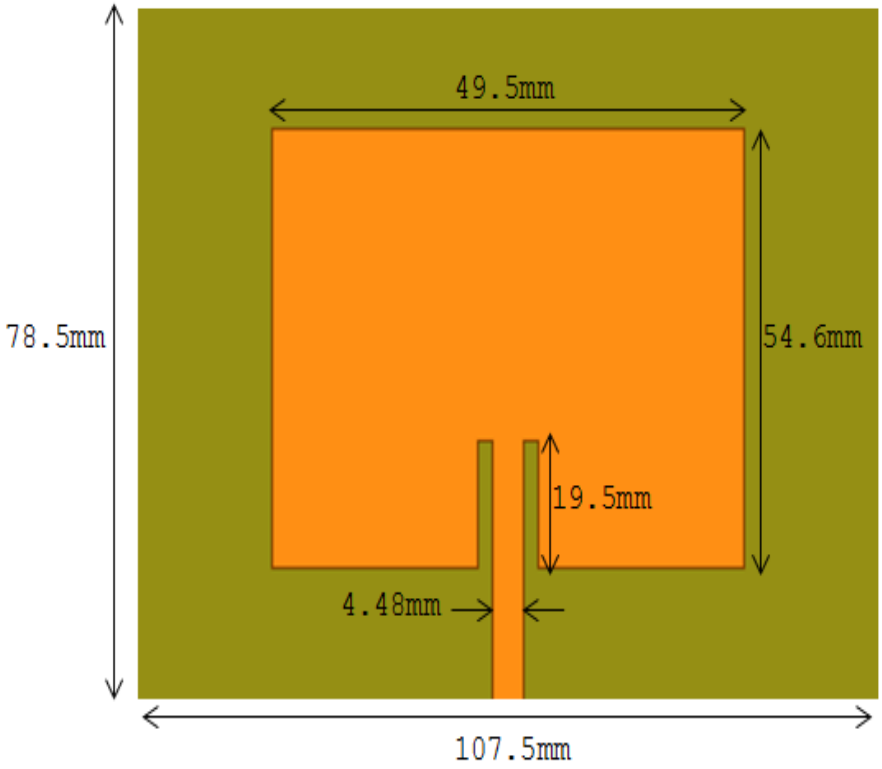

Figure 4.1 The geometry and dimension of the single element microstrip patch antenna.

The patch shown in **Figure 4.1** was modeled and simulated using Ansys HFSS. Simulated $|S_{11}|$(dB) data are shown in **Figure 4.2**. It is clear that the resonant frequency of the patch is about 2 GHz. It exhibits a very narrow bandwidth, as expected considering a -10 dB limit for the $20\log_{10}|S_{11}|$.

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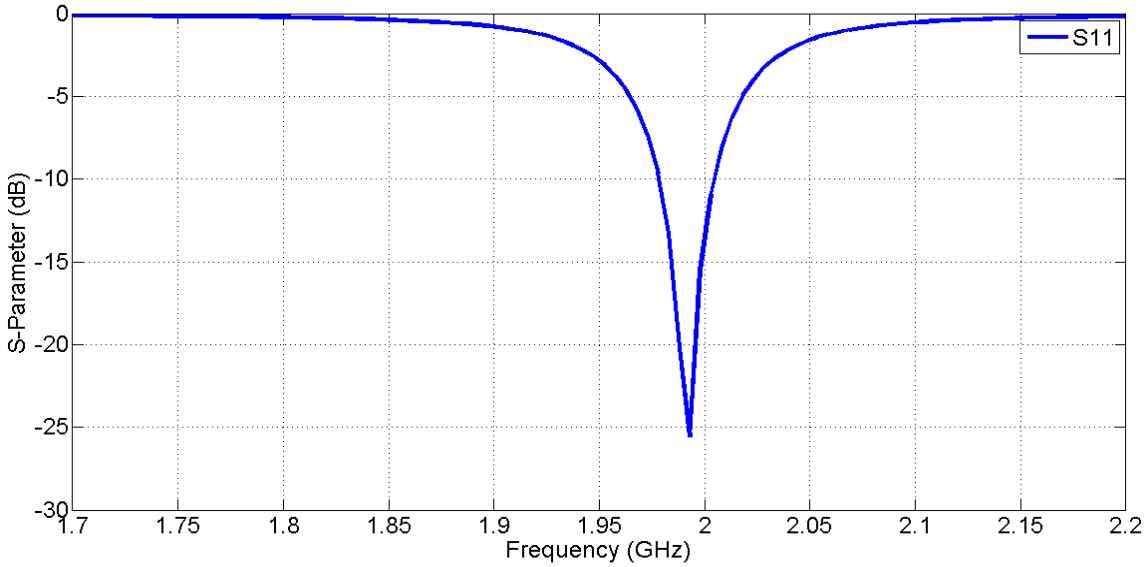

Figure 4.2 Simulated $|S_{11}|$ data of the microstrip patch antenna in dB.

Simulated VSWR data are plotted in **Figure 4.3.**

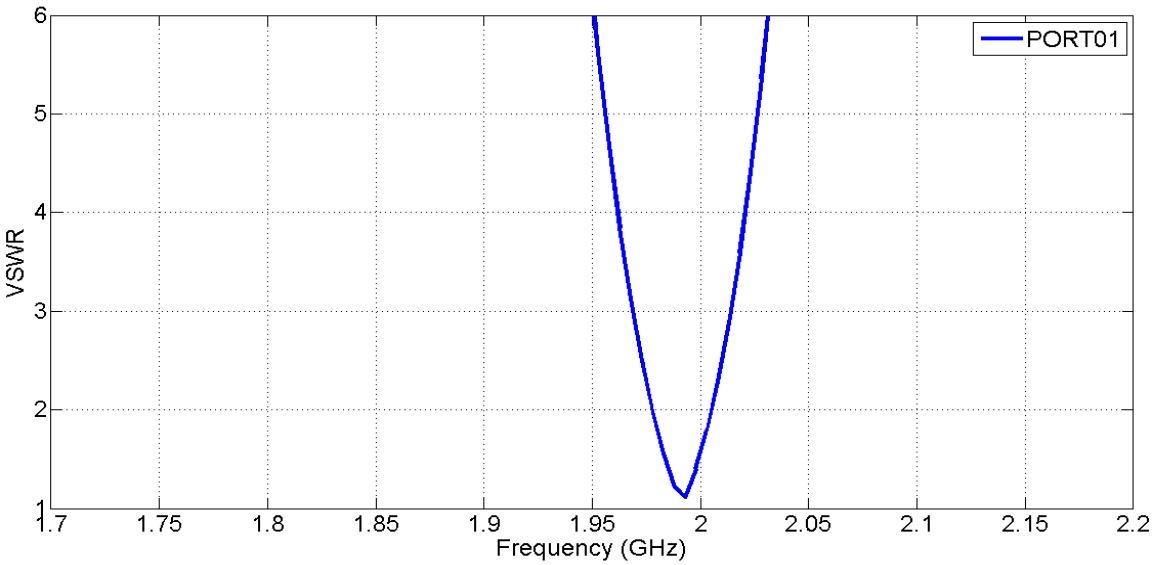

Figure 4.3 Simulated VSWR of the single element patch on Duroid 5880.

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Radiation patterns in both the E and H planes are shown in **Figure 4.4.**

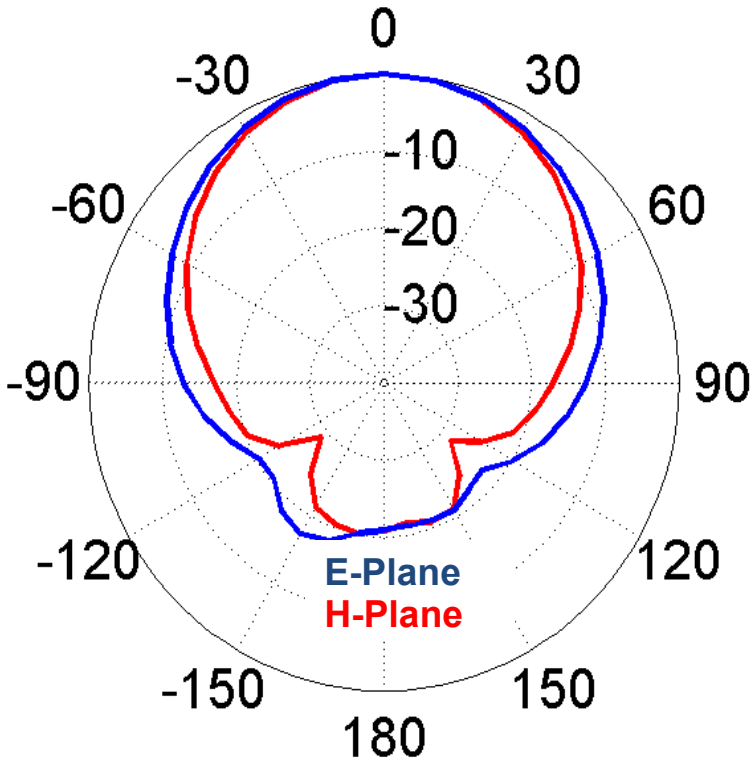

Figure 4.4 Simulated radiation patterns of the patch antenna on Duroid 5880. Peak gain=8 dBi.

4.2 Microstrip Patch Phased Array

A four-element microstrip patch phased array was considered with a 2 GHz operation frequency. The four patches will be along a straight line making it a linear array. The desired beam scanning angles (θ_0) are 35˚, 20˚, 0˚, -20˚ and -35˚.

In order to scan the beam along each of the angles mentioned above we have to analytically determine the

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progressive phase shift β that will be required. Note that β is given by[7].

$$\beta = -k\, d\, cos\theta_0$$

Table 4.2 The progressive phase shift for each scanning angle at each port.

Scanning angle θ_0	**Port01 β**	**Port02 β**	**Port03 β**	**Port04 β**
35˚	0˚	-125˚	-250˚	-375˚
20˚	0˚	-72˚	-144˚	-216˚
0˚	0˚	0˚	0˚	0˚
-20˚	0˚	72˚	144˚	216˚
-35˚	0˚	125˚	250˚	375˚

The four-element patch array designed and simulated using HFSS, is shown in **Figure 4.5.**

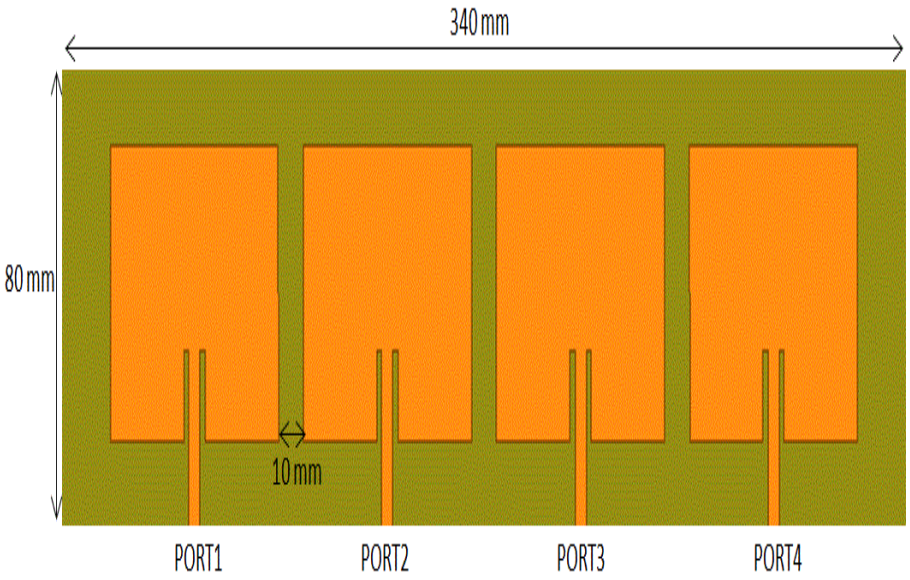

Figure 4.5 The four-element patch array model in HFSS.

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Before implementing the phased array design consisting of the delay lines to create the phase delays, the patch array was simulated considering four separate ports or feed arrangements as shown in **Figure 4.5**. The S-parameters of this patch array are shown in **Figure 4.6**. As seen, the mutual coupling between the individual elements is always <12dB. Further reduction in mutual coupling will require the inter-element spacing to be increased. Simulated radiation patterns are shown in **Figure 4.7**.

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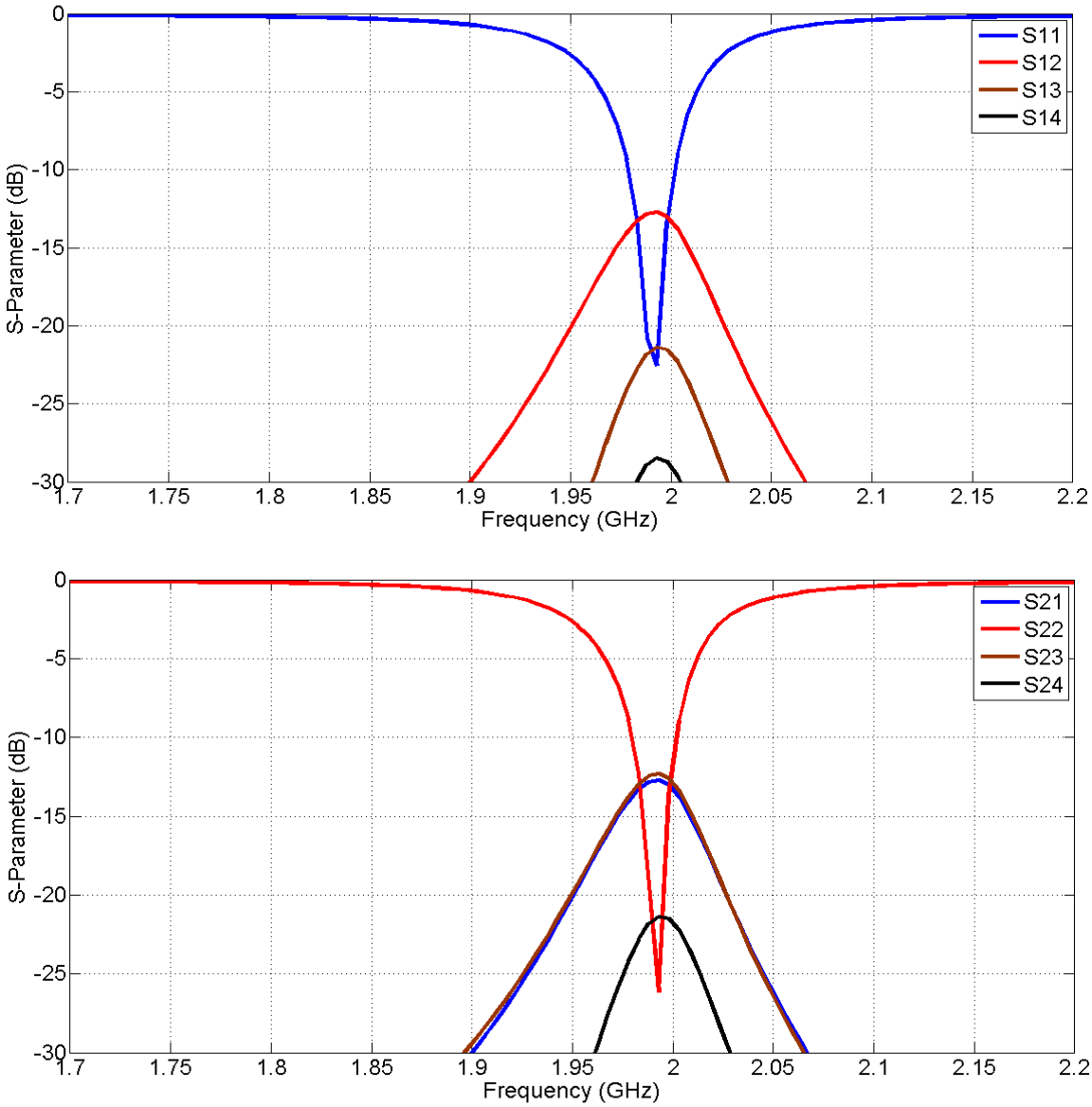

Figure 4.6 Simulated S-Parameters of the patch array (continue next page).

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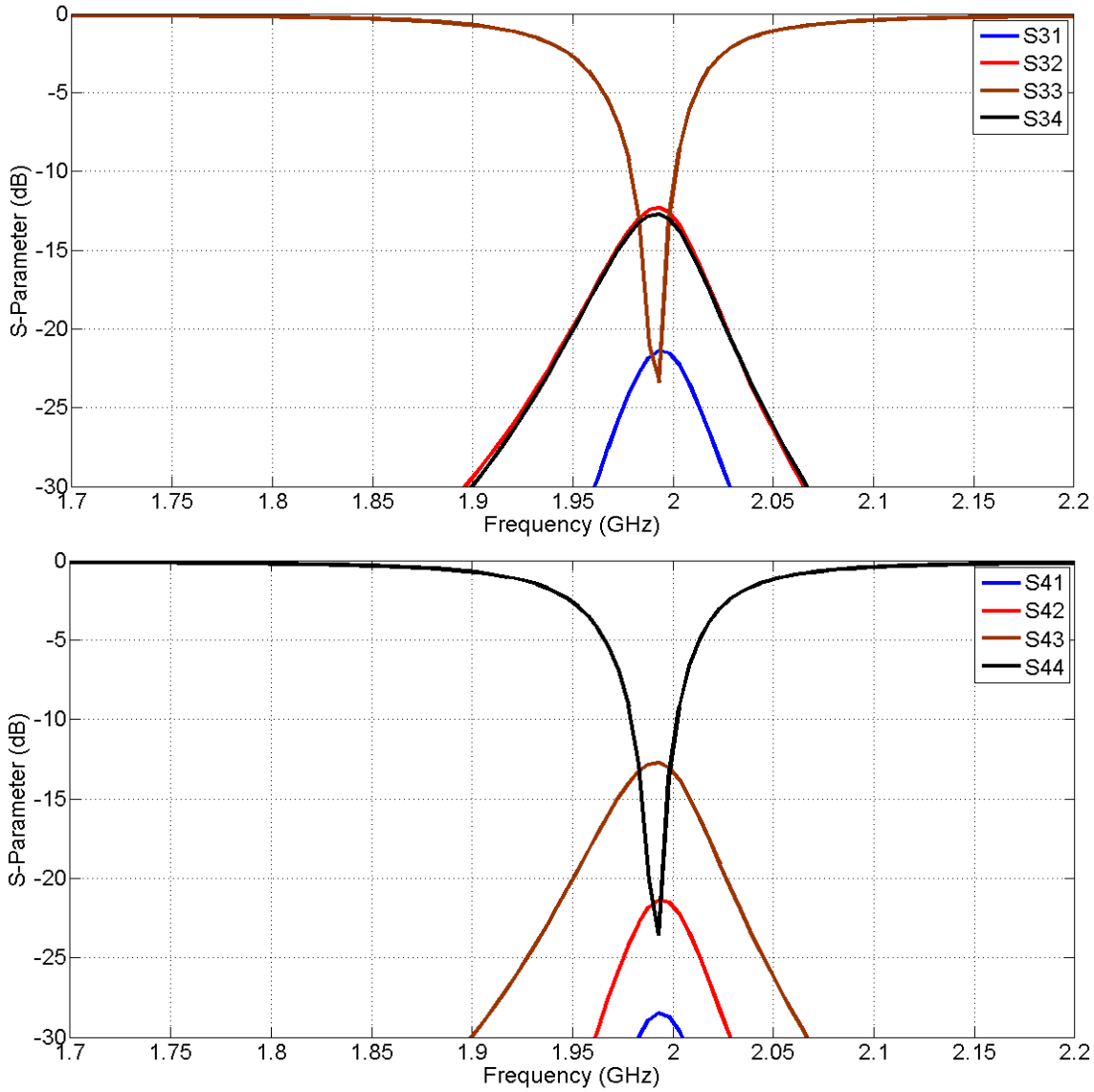

Figure 4.6 Simulated S-parameters of the patch array.

Comparing the patterns of **Figure 4.7** with that shown in **Figure 4.4,** it is clear that the array is more directive. The array has higher gain compared to the single element antenna (11.6 dBi compared to 8 dBi).

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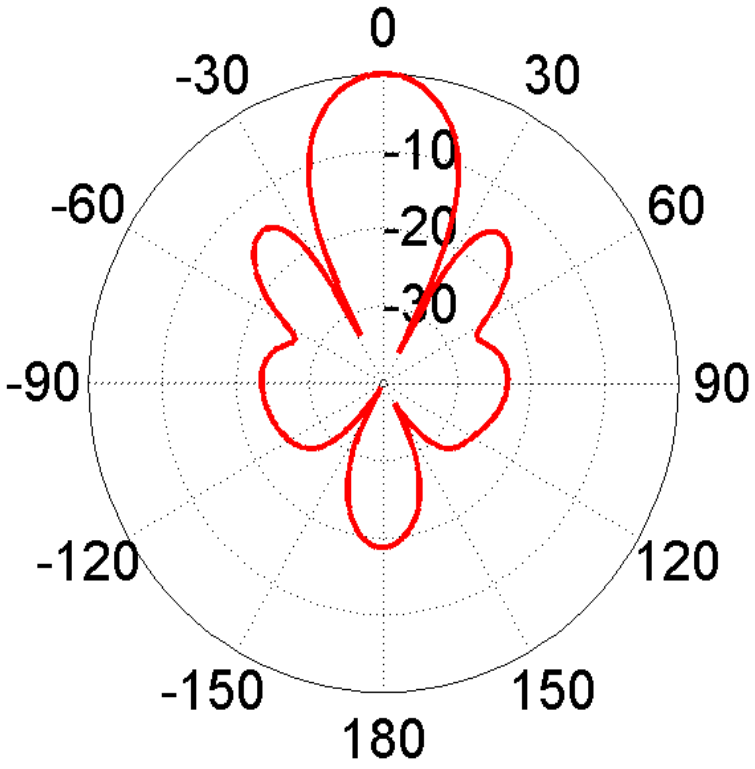

Figure 4.7 Simulated radiation pattern of the patch array with the main beam formed at zero degree. Peak gain=11.6 dBi.

Next, simulations were performed to investigate the beam scanning aspects of the phased array. To do that the scheme illustrated in **Figure 4.8** was followed. To scan the beam along a desired angle θ_0 a set of β values were used to excite each antenna element. This was done by changing the β for each element in HFSS. For example, to scan the beam along θ_0=0˚ direction, β was set to 0 for all elements while for θ_0=35˚ direction, β was progressively decreased by a factor of -125 as shown in **Table 4.2** and **Figure 4.8**. Thus in total five simulations were performed for scanning the

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beam along θ_0 = 0˚,20˚,35˚,-20˚ and -35˚ directions. The radiation patterns shown in **Figure 4.9** to **Figure 4.12** represent the patterns of the five simulations.

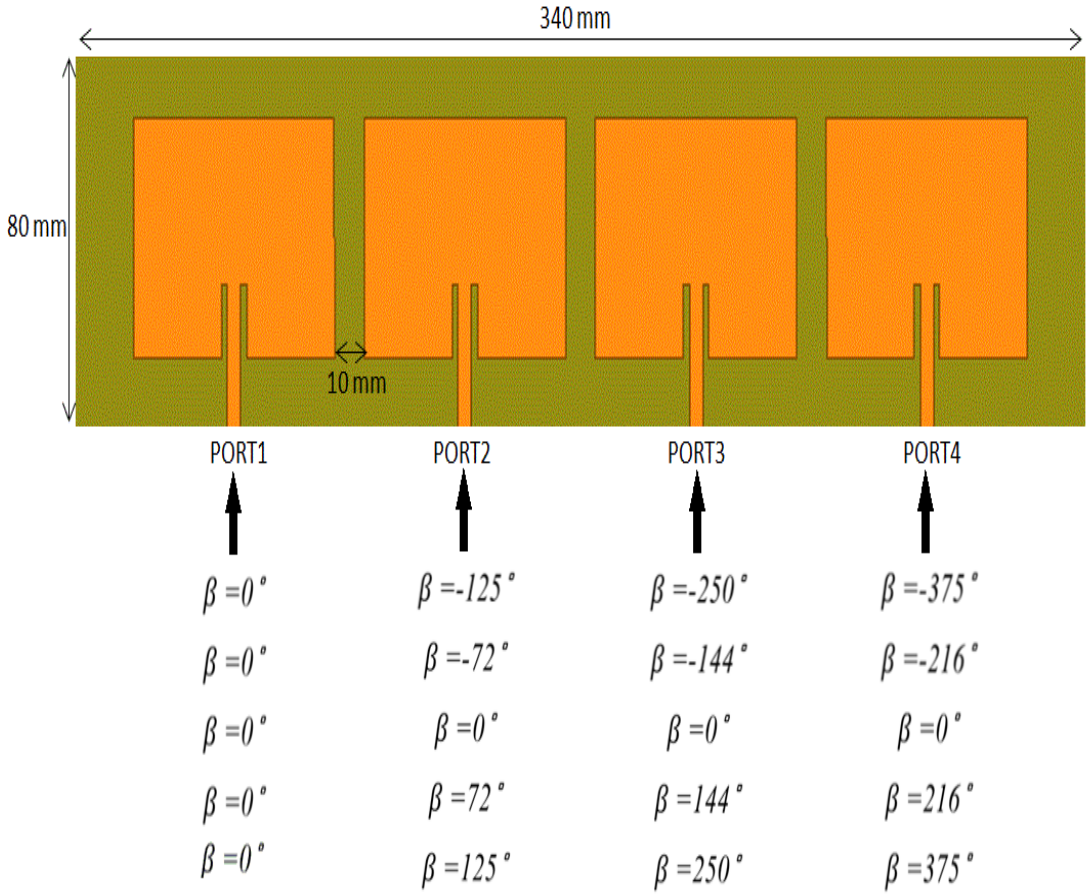

Figure 4.8 Progressive phase shift $\boldsymbol{\beta}$ required to scan the beam along $\boldsymbol{\theta_0}$ = 0˚,20˚,35˚,-20˚ and -35˚ directions.

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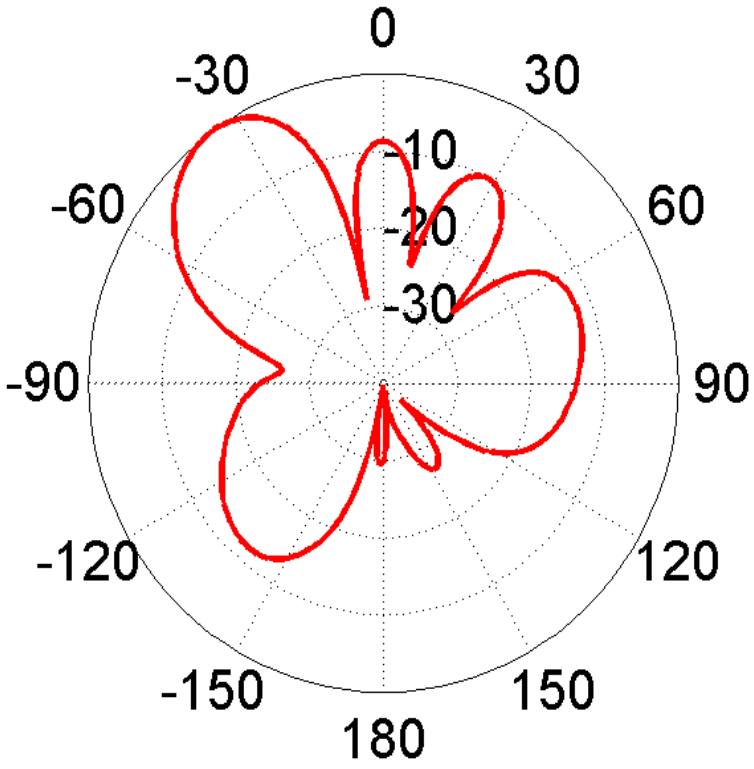

Figure 4.9 Beam scanning at $\boldsymbol{\theta_0}$=-35 degrees. Peak gain=10.7 dBi.

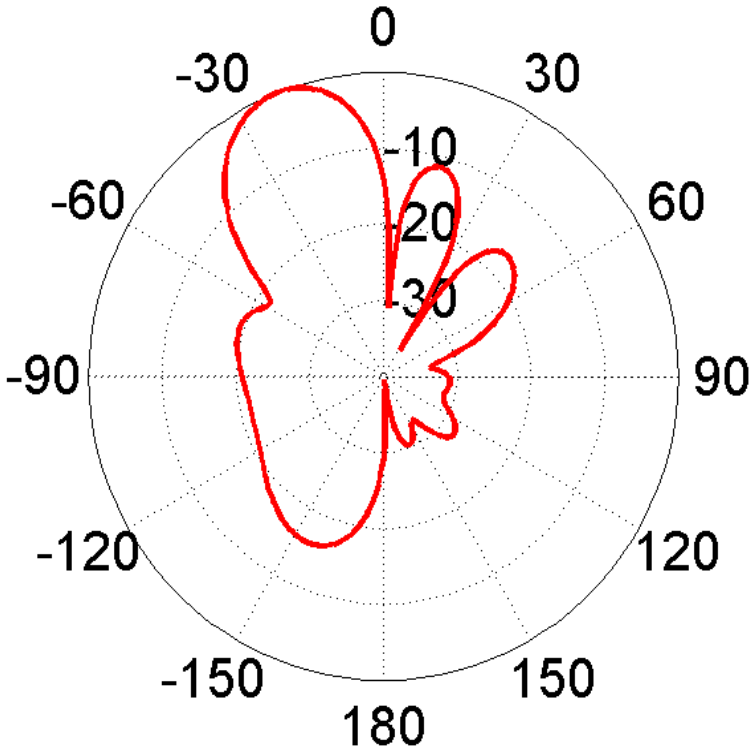

Figure 4.10 Beam scanning at $\boldsymbol{\theta_0}$=-20 degrees. Peak gain=11.7 dBi.

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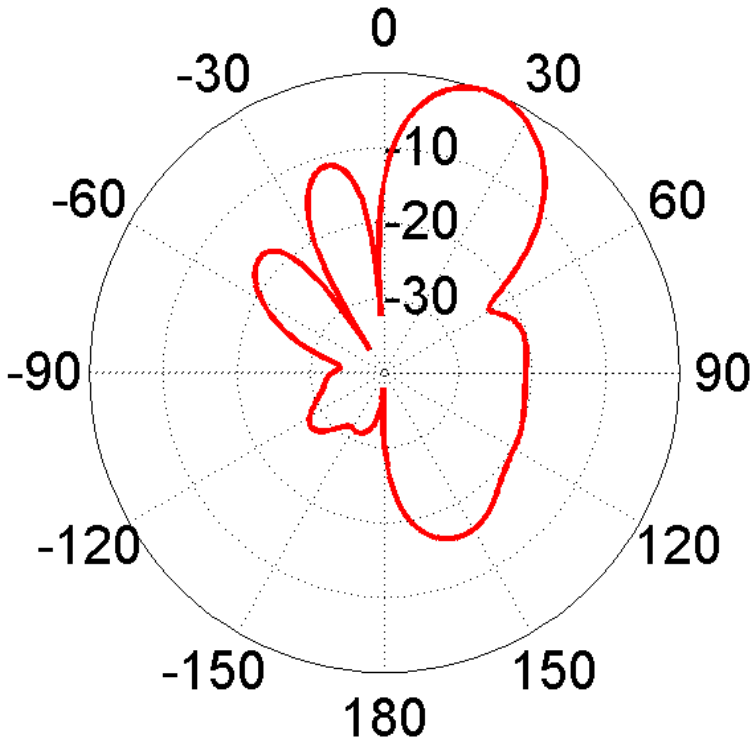

Figure 4.11 Beam scanning at $\boldsymbol{\theta_0}$=20 degrees. Peak gain=11.6 dBi.

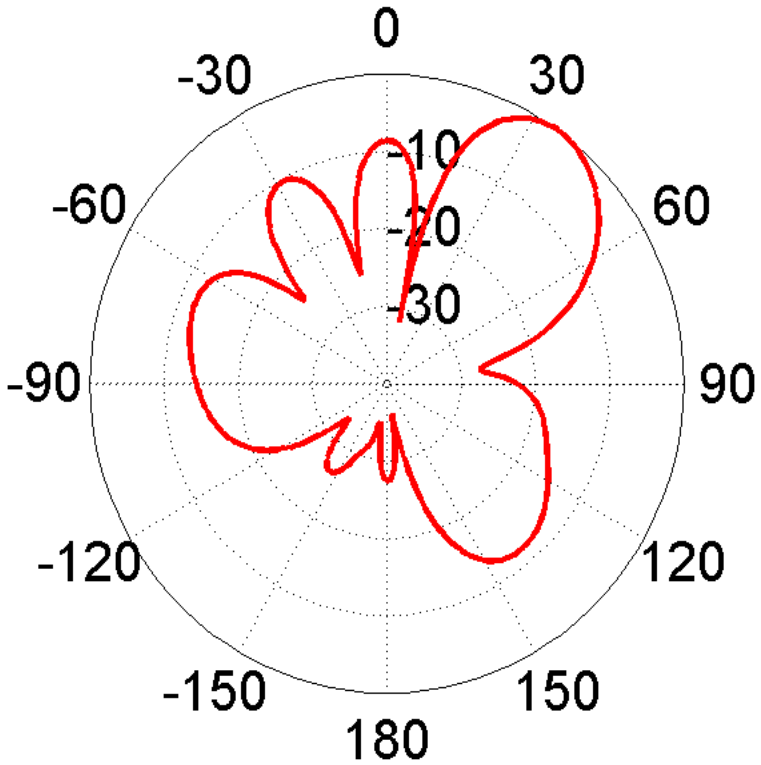

Figure 4.12 Beam scanning at $\boldsymbol{\theta_0}$=35 degrees. Peak gain=10.7 dBi.

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These results show how changing β could allow us scan the main beam along different angles without physically moving or rotating the antenna array.

4.3 Phase Delay Lines Design.

In order to implement the progressive phase shift β described in **Table 4.2** phase delay lines are required. Typically the delay is given by the product of the phase constant and the electrical length of the line. Examining **Figure 4.13** would reveal the different paths the signal could travel to have the required phase shift.

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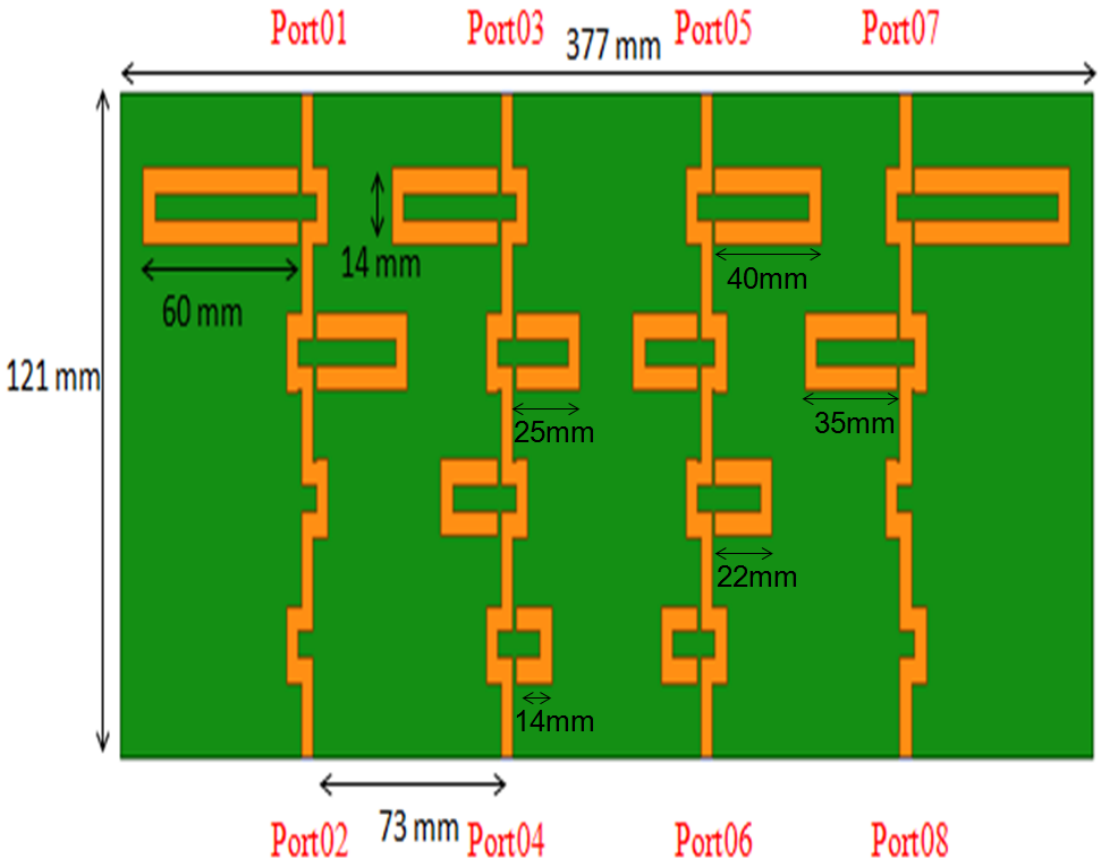

Figure 4.13 Proposed design of microstrip phase delay lines.

The spaces between the microstrip traces will accommodate GaAs Single Pole Double Throw (SPDT) switches [9] to switch the delay from one value to another. We chose GaAs switches for their easy availability and implementation. Nevertheless, PIN diode, GaN or MEMs switches can also be used. Clearly the different lengths of the microstrip U-shaped loops along with different switching combinations in **Figure 4.13** will provide different phase delays resulting in the progressive phase shift β required for that specific

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beam scanning angle $\boldsymbol{\theta_0}$. For example, the scheme shown in **Figure 4.13** represent β=0 which will result in the beam being directed in the θ_0=0 degree direction.

The specific phase delay created by each U-shaped microstrip segment is shown in **Figure 4.14.**

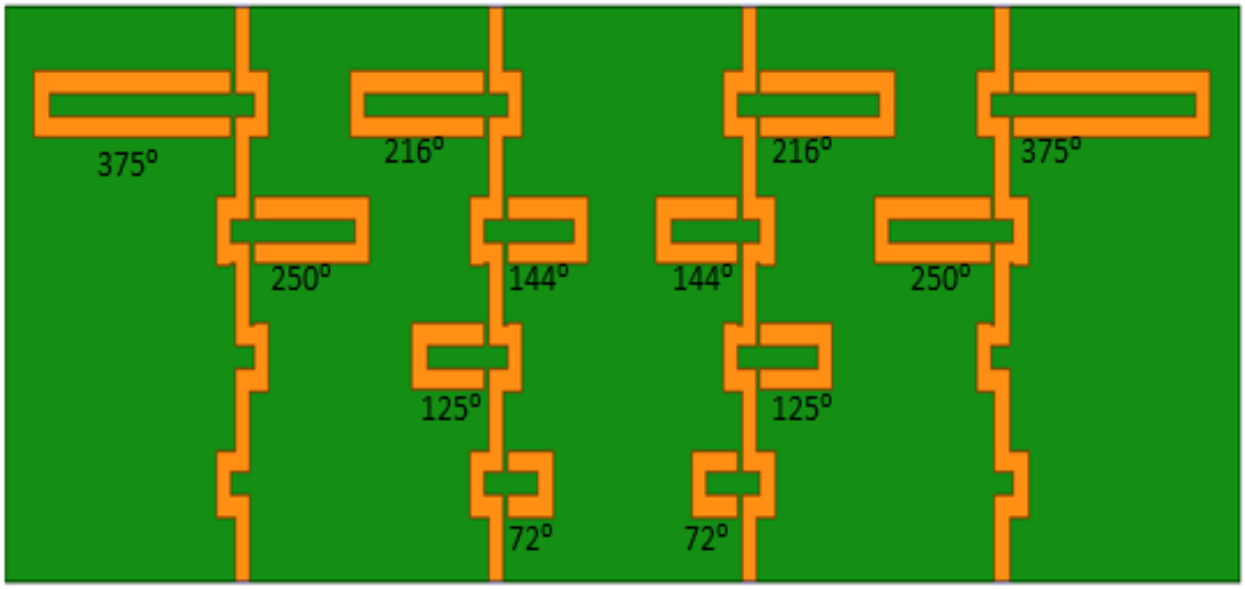

Figure 4.14 Illustration of the phase delay created by the microstrip U-shaped delay segments.

Shown in **Figure 4.15** to **Figure 4.17** are the simulated progressive phase shifts for each β.

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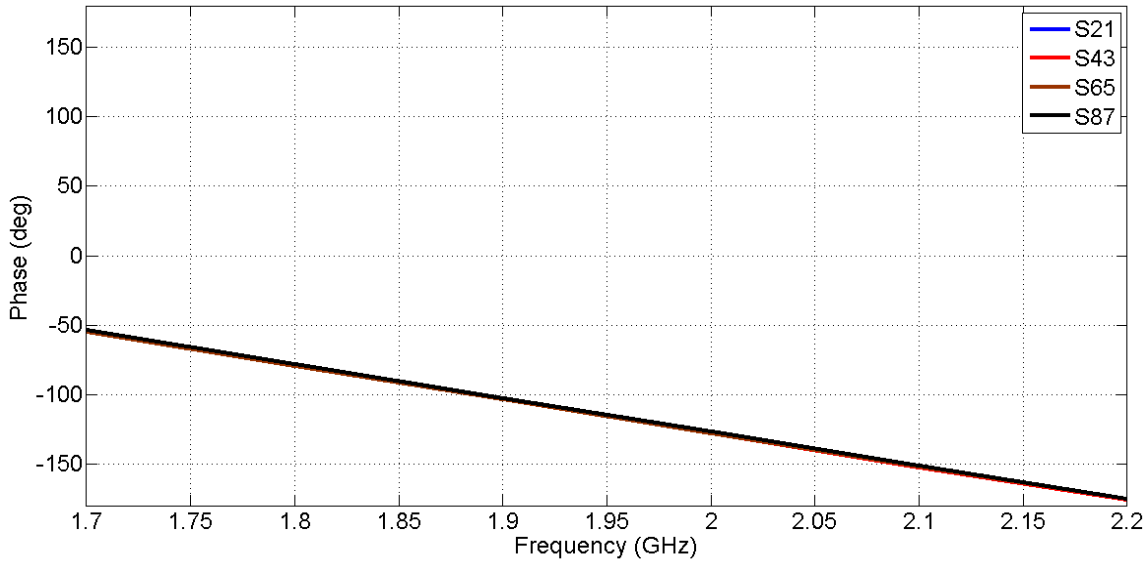

Figure 4.15 Simulated progressive phase shift $\boldsymbol{\beta}$=0 degree for each feed transmission line.

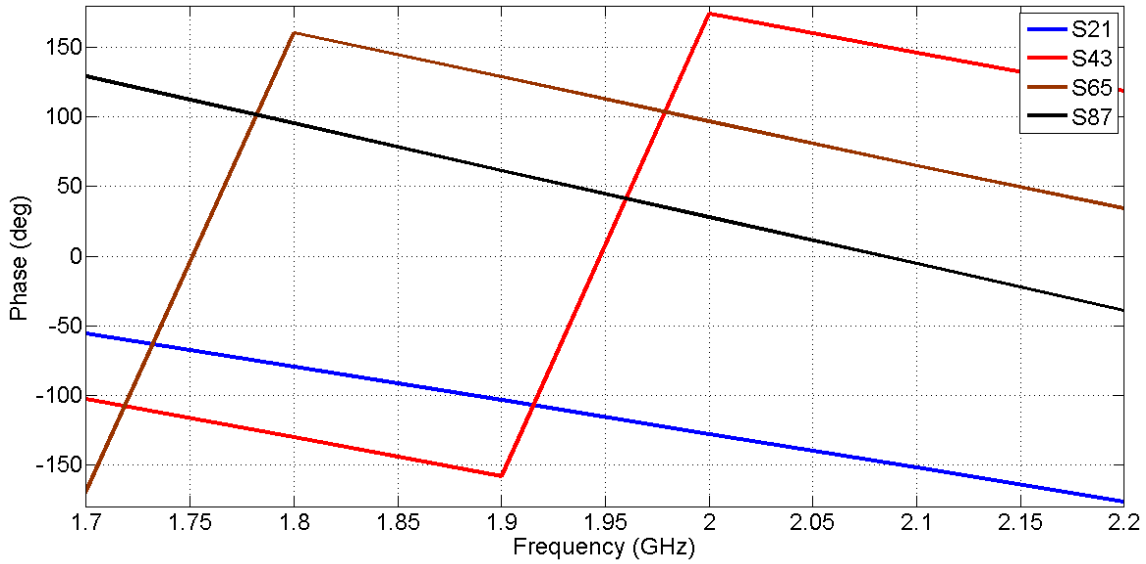

Figure 4.16 Simulated progressive phase shift $\boldsymbol{\beta}$=72 degree for each feed transmission line.

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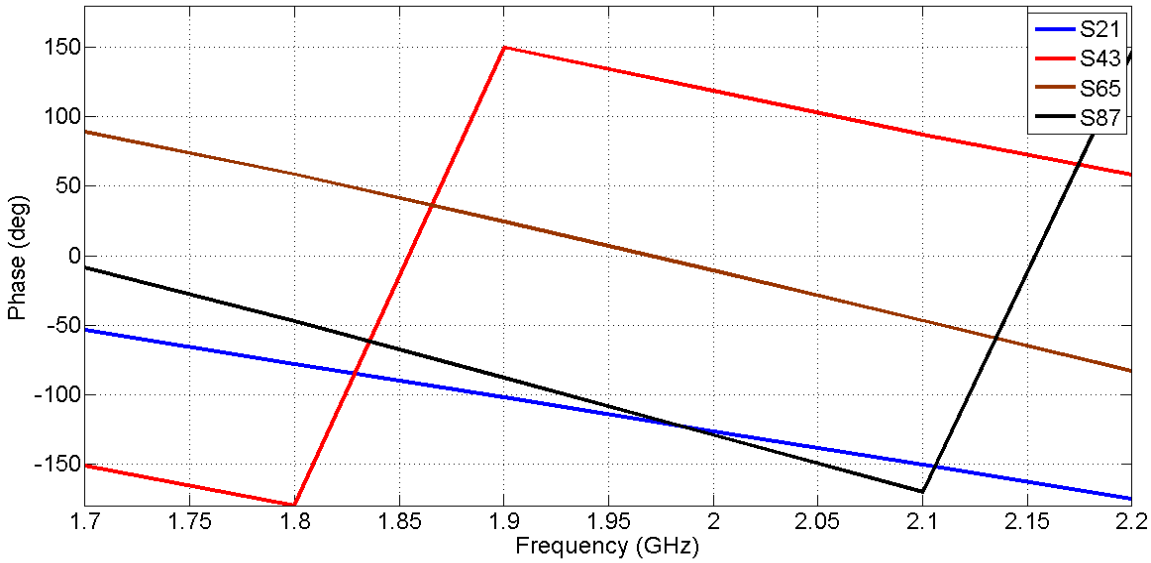

Figure 4.17 Simulated progressive phase shift $\boldsymbol{\beta}$=125 degree for each feed transmission line.

After that we incorporated the delay lines design with corporate feeding to have a single source input. The design of the delay lines with corporate feed is shown in **Figure 4.18.**

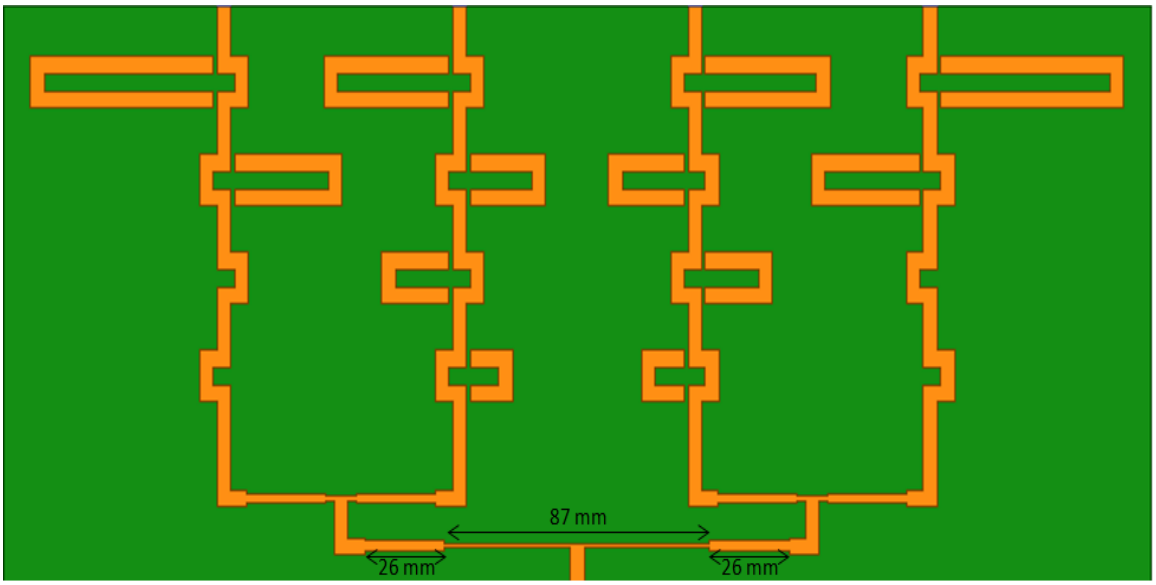

Figure 4.18 Delay lines with corporate feed.

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The results of the simulated design of the corporate feed with the delay lines are shown in **Figure 4.19** to **Figure 4.21.**

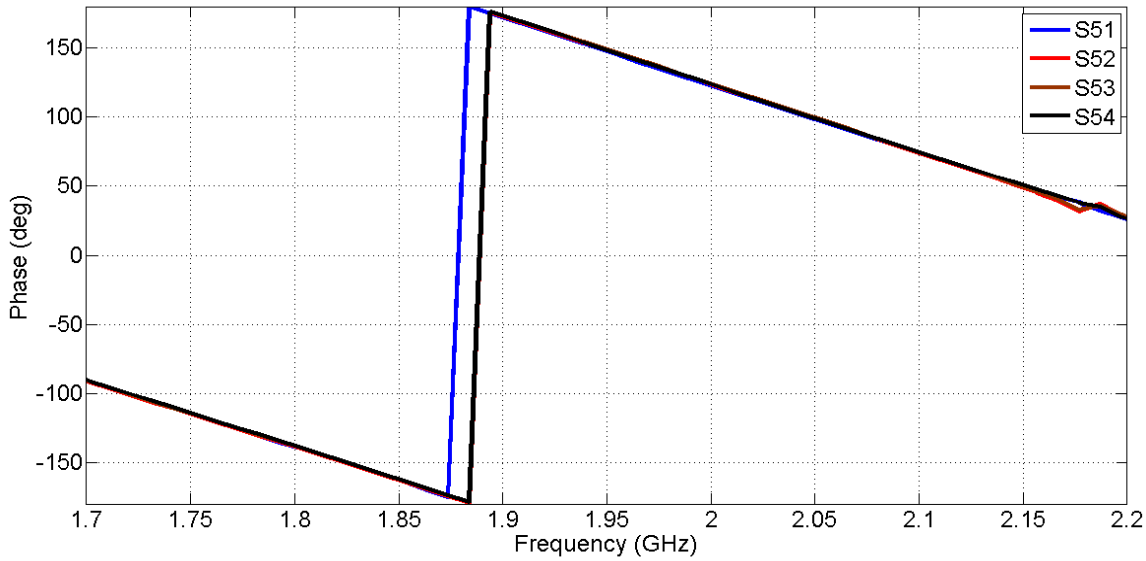

Figure 4.19 Progressive phase shift $\boldsymbol{\beta}$ of the delay lines of 0 degree.

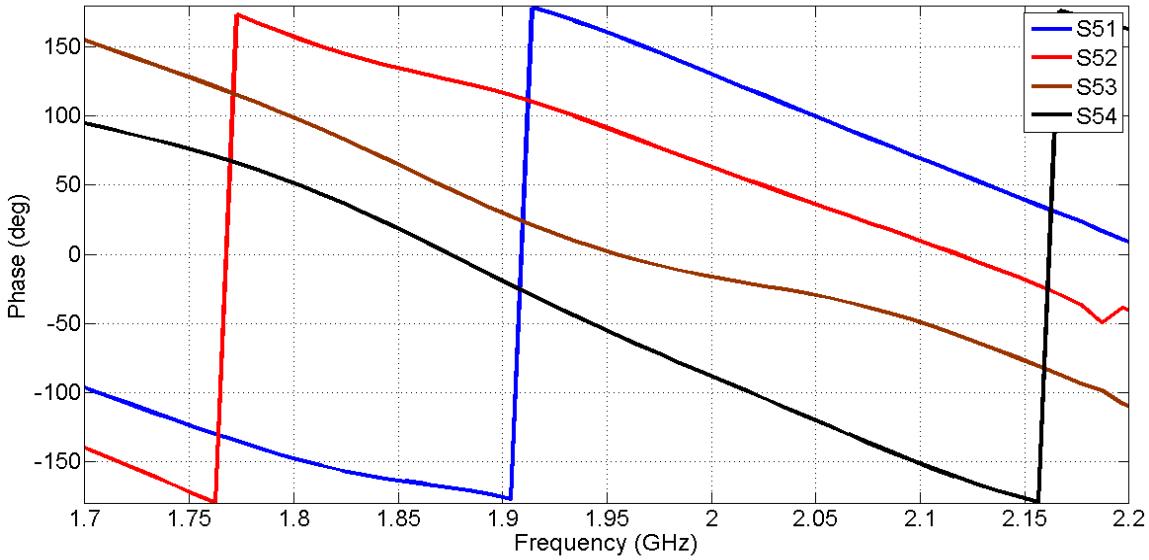

Figure 4.20 Progressive phase shift $\boldsymbol{\beta}$ of the delay lines of 72 degree.

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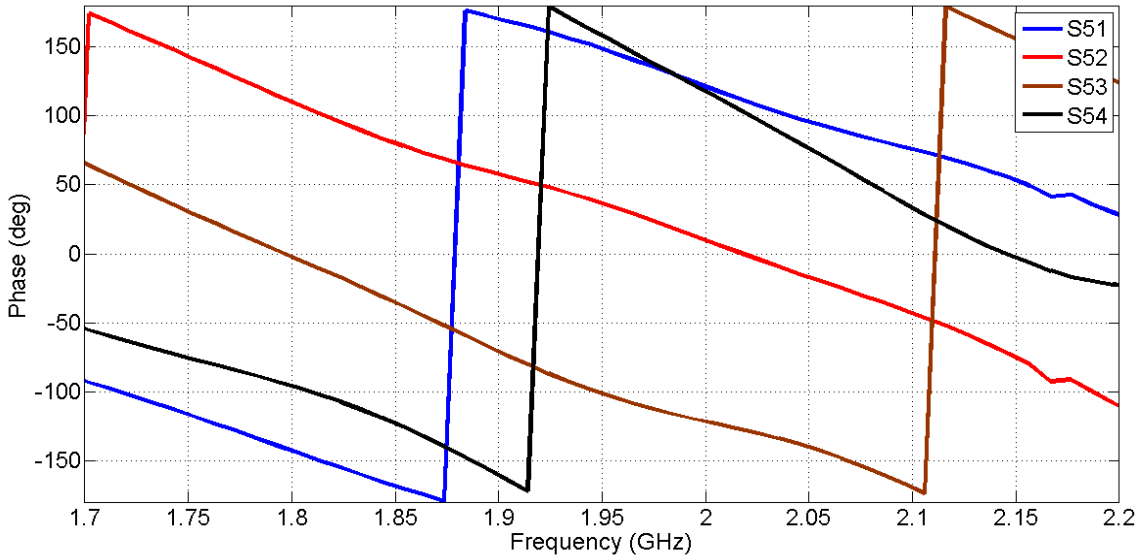

Figure 4.21 Progressive phase shift $\boldsymbol{\beta}$ of the delay lines of 125 degree.

4.4 Complete Design and Simulation of the Array.

Implementing the delay lines with the corporate feeding into the main model, as shown in **Figure 4.22**, would introduce losses.

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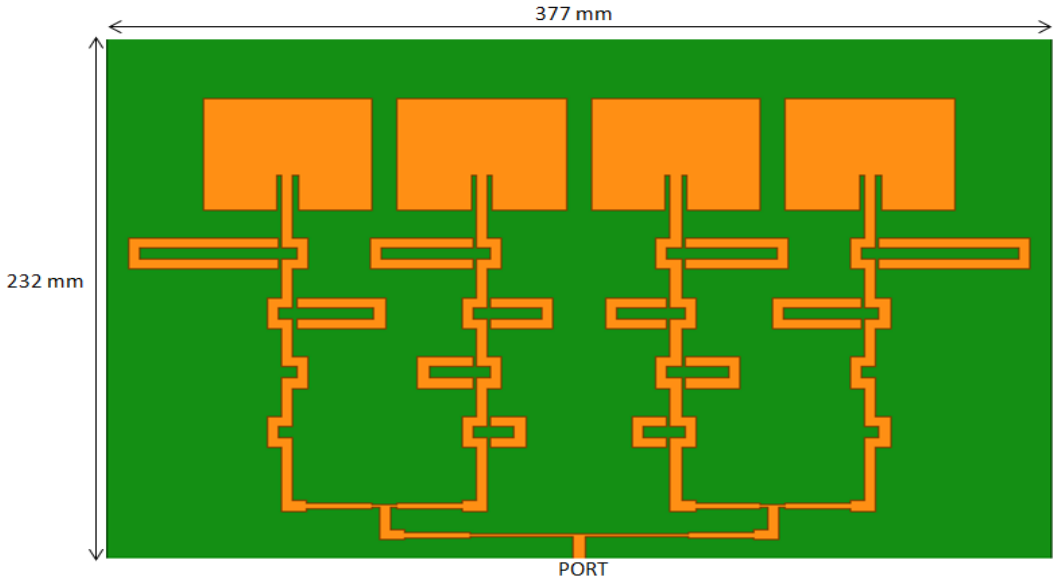

Figure 4.22 Four element patch antenna array with delay lines and corporate feed.

The signal has to travel longer path lengths in order to provide the proper delay; this will be one of the losses in the system. The simulated radiation patterns for the array are shown in **Figure 4.23** to **Figure 4.25.**

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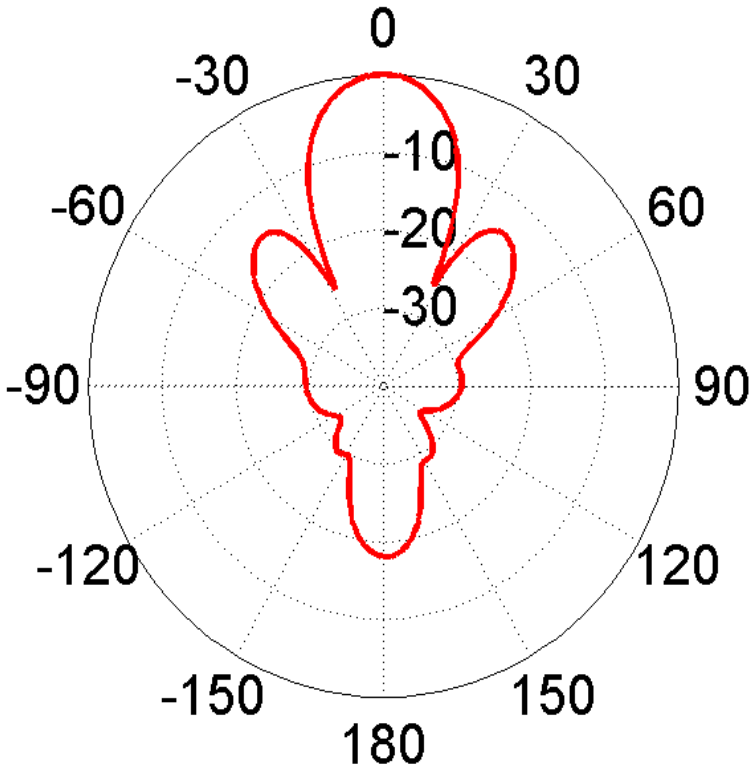

Figure 4.23 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=0 degree. Peak gain=12.5 dBi.

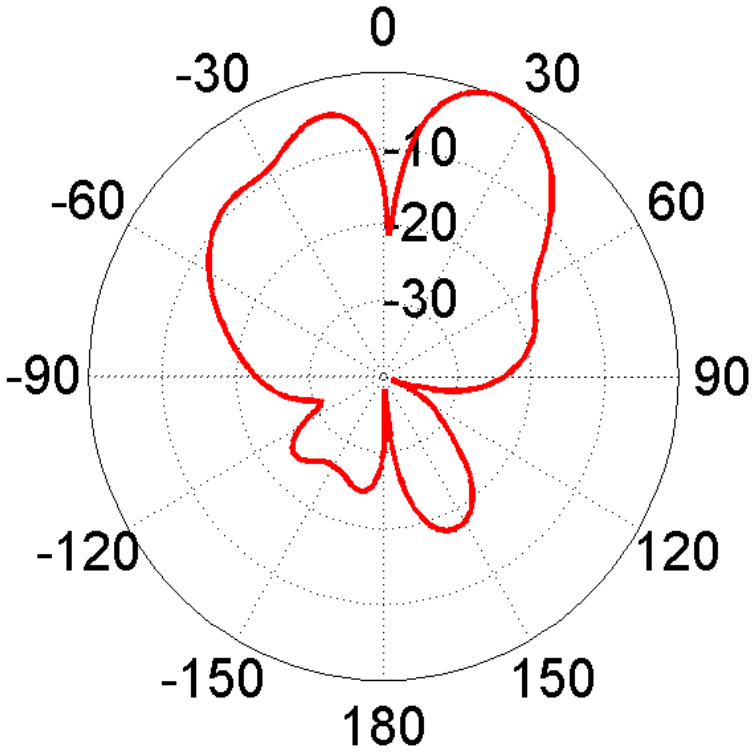

Figure 4.24 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=20 degree. Peak gain=10.9 dBi.

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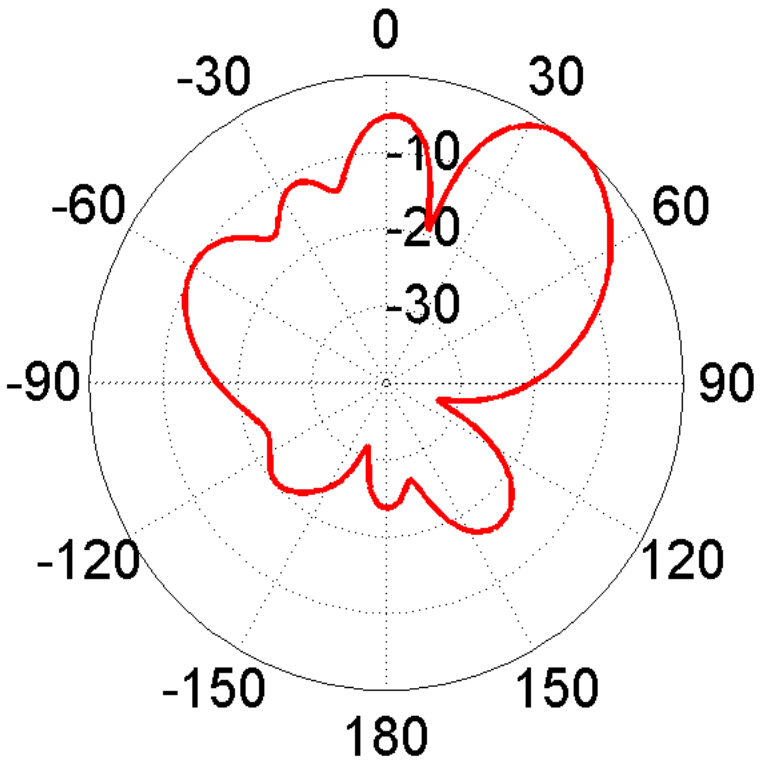

Figure 4.25 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=35 degree. Peak gain=10.8 dBi.

It is clear that the radiation patterns shown in **Figure 4.23** to **Figure 4.25** do their jobs in terms of directing the beam along the desired directions. However, there are side lobes that are at higher intensity than they were in the patterns without the delay lines. These discrepancies might be caused by the losses in the transmission lines.

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4.5 Single Stage Phase Shifter Network Prototype

In order to fabricate the full design of the phase shifter network we started by modeling and fabricating a single stage phase shifter prototype to allow us study and analyze the model in a simpler manner. We designed the prototype to have the main beam in the radiation pattern scan between $\theta_0 = 0^\circ$ and $\theta_0 = -20^\circ$. Shown in **Figure 4.26** is the single stage phase shifter model designed in HFSS. As seen the line lengths are the same and thus β=0 degree. But as the switches will be turned on to activate the U-shape sections β will assume values of 72˚, 144˚, and 216˚ respectively.

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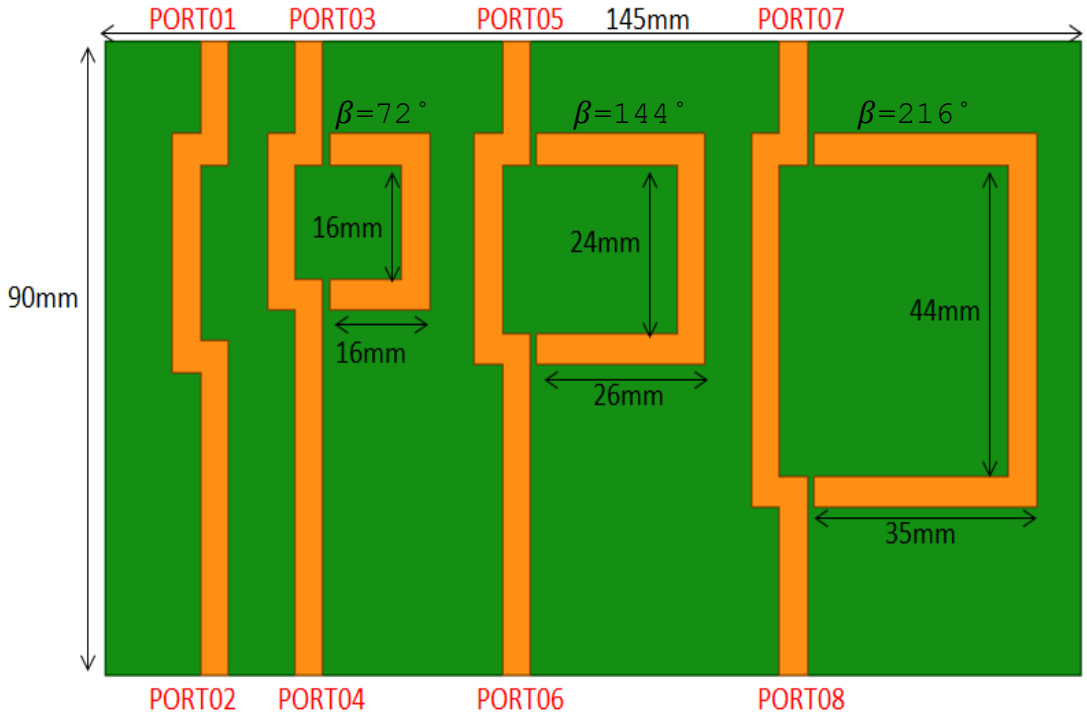

Figure 4.26 Phase shifter network to steer the beam in $\boldsymbol{\theta_0 = 0^\circ}$ **and** $\boldsymbol{\theta_0 = -20^\circ}$**.**

Shown in **Figure 4.27** and **Figure 4.28** are the simulated progressive phase shifts for β=0° and β=72°.

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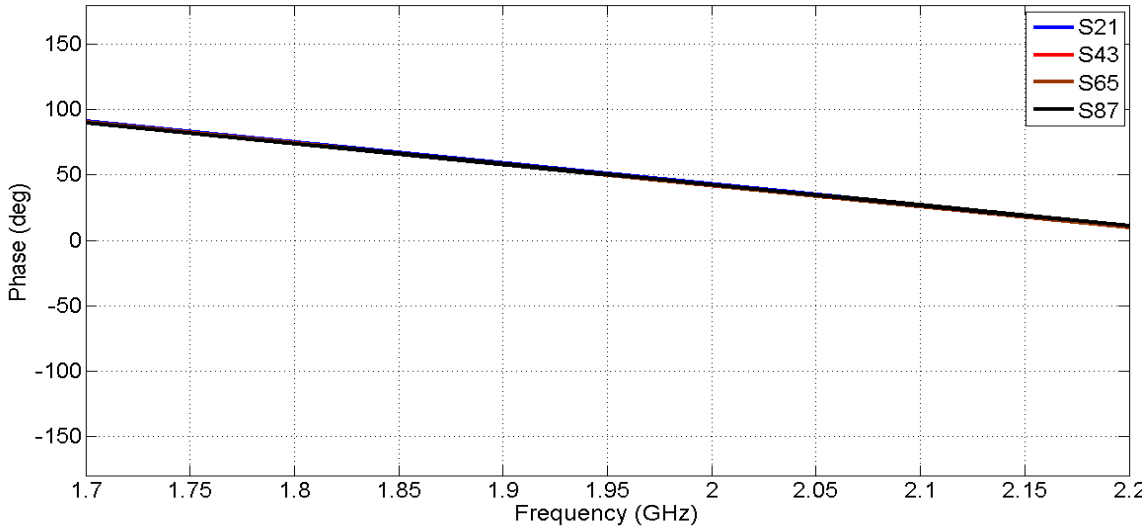

Figure 4.27 Progressive phase shift β of the delay lines for β=0 degree.

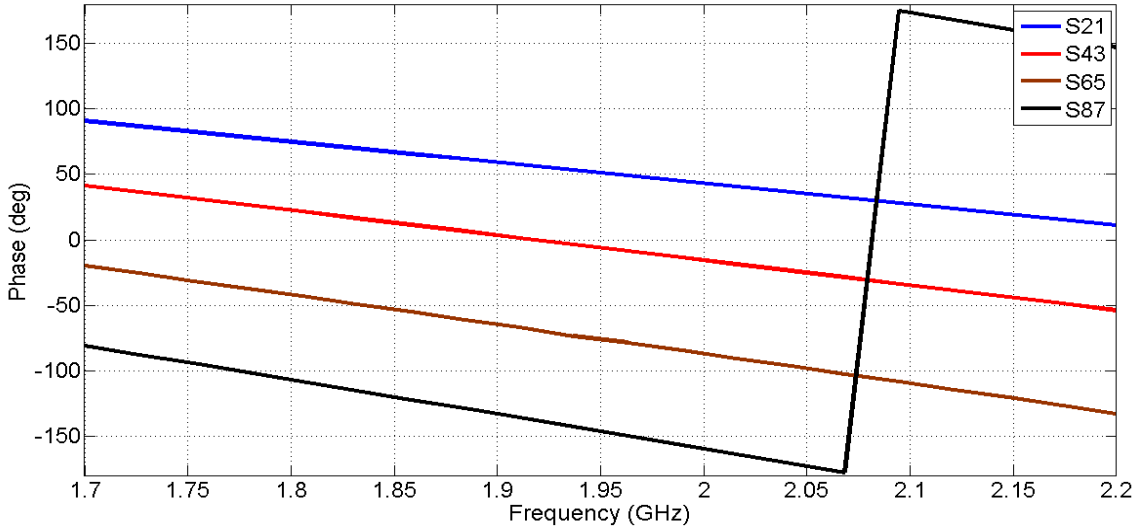

Figure 4.28 Progressive phase shift β of the delay lines for β=72 degrees.

The single stage phase shifter was fabricated consisting of GaAs SPDT switches[9]. The DC to 3 GHz switches were manufactured by a company called Hittite, The switch has

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low insertion loss (0.3-0.9 dB), high isolation (27 dB), and high return loss (21 dB), as shown in **Table 4.3**.

Table 4.3 Switch characteristics.

Switch Type	**GaAs SPDT SWITCH**
Working Frequency	DC - 6 GHz
Insertion Loss	0.3-0.9 dB
Isolation	27 dB
Return Loss	21 dB
Maximum RF Input Power	+34 dBm
Control Voltage Range	-0.2 to +12 Vdc

The delay lines were fabricated on a 1.55 mm thick Duroid 5880 substrate. A photograph of the prototype single stage phase shifter is shown in **Figure 4.29**.

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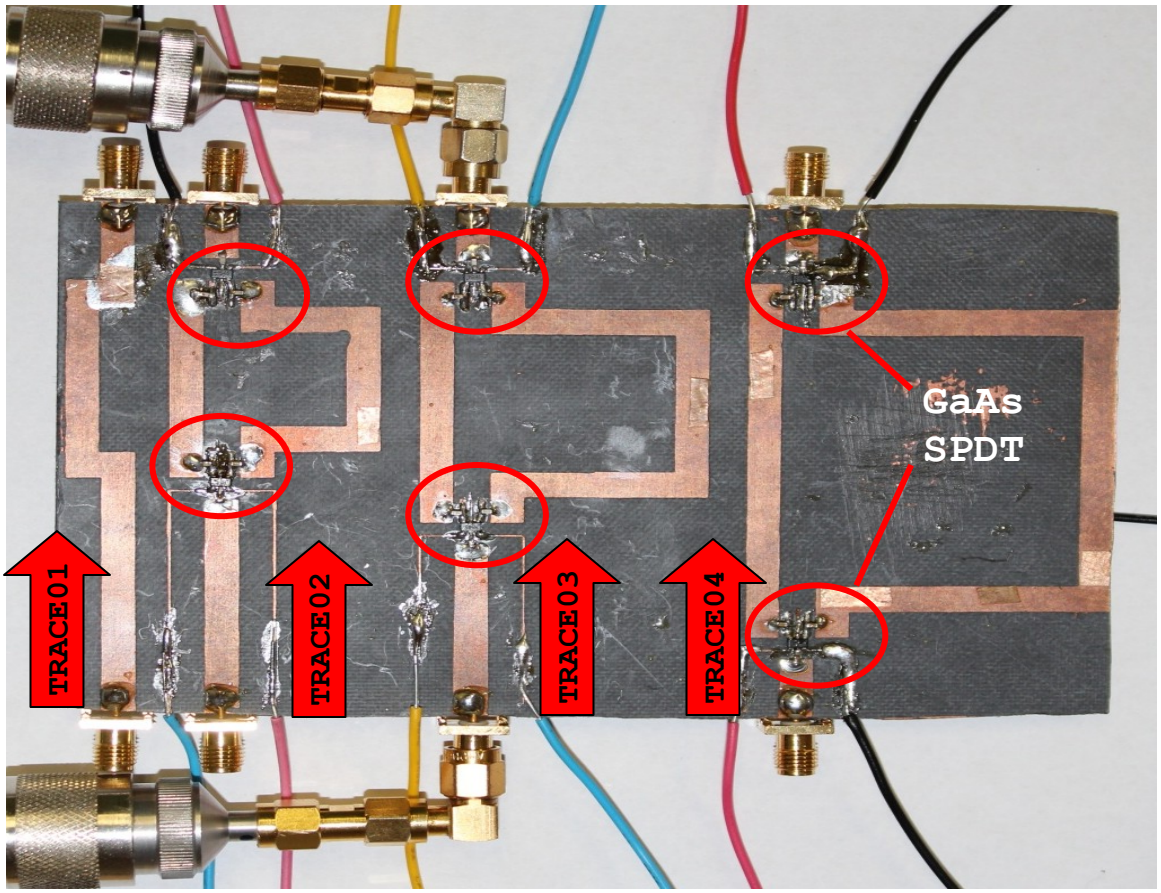

Figure 4.29 Photographs of fabricated single stage phase shifter containing GaAs SPDT switches.

An Agilent Vector Network Analyzer (VNA) was used to take the S-parameter measurements that reflected the insertion loss, return loss, and the phase delay. The S-parameter measurements are captured in **Figure 4.30** to **Figure 4.33.**

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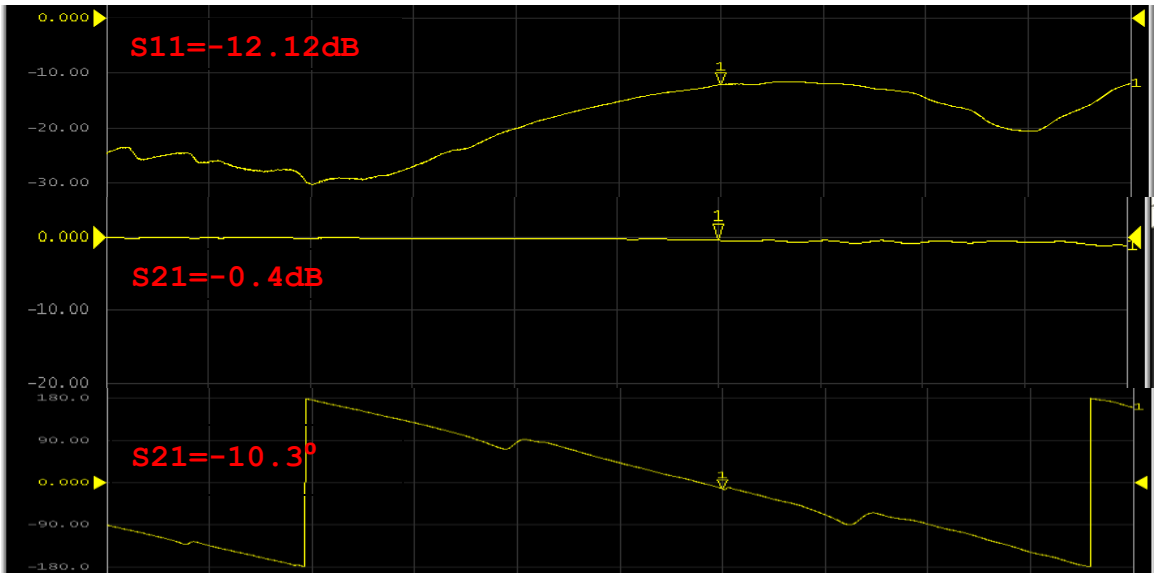

Figure 4.30 Measured S-parameter at Trace01

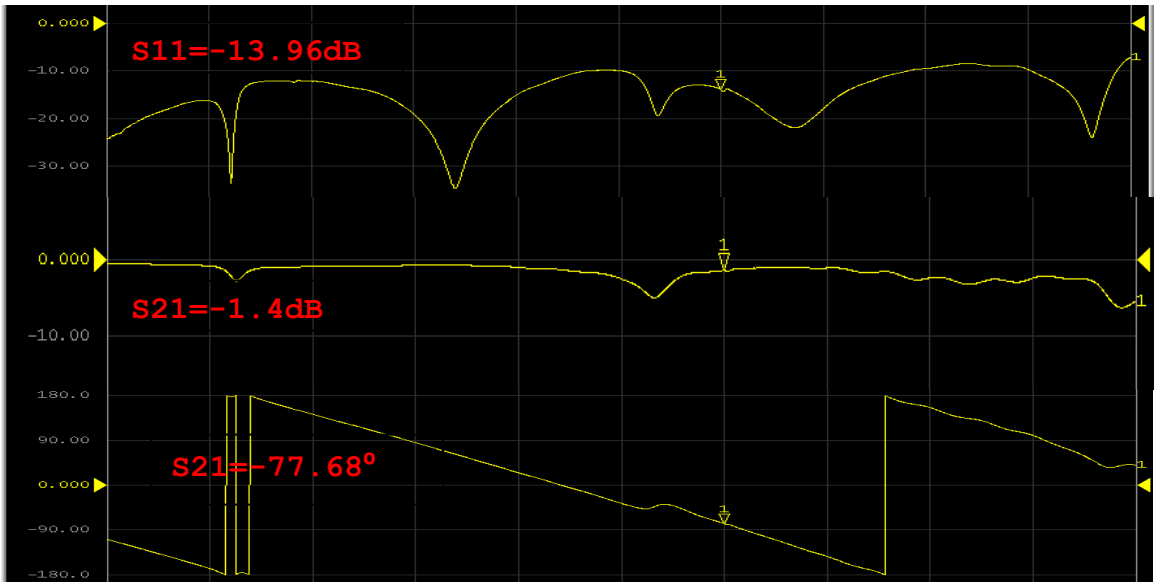

Figure 4.31 Measured S-parameter at Trace02

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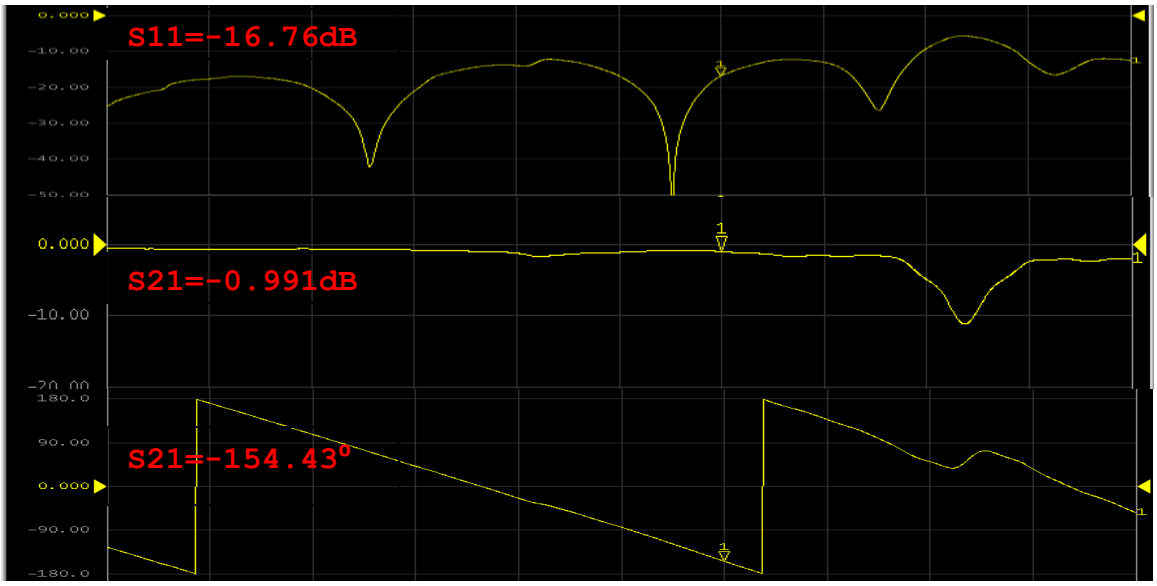

Figure 4.32 Measured S-parameter at Trace03

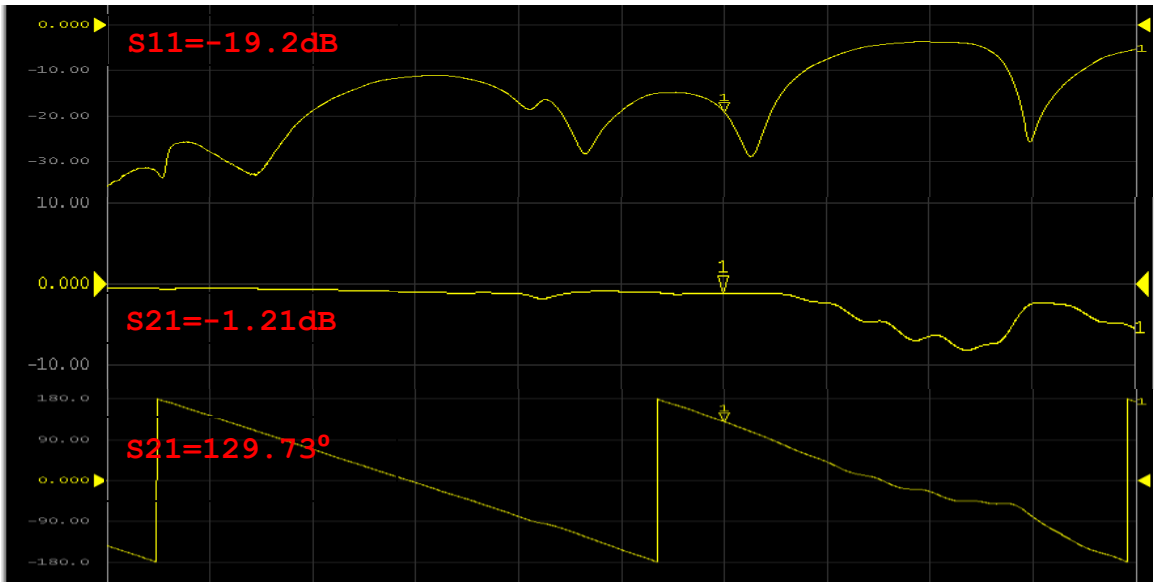

Figure 4.33 Measured S-parameter at Trace04

The single stage phase shifter, according to the plots above, shift the phase progressively by approximately $\beta=72^{o}$. In the first trace $\beta=-10.3^{o}\approx 0^{o}$, second trace $\beta=-77.68^{o}\approx -72^{o}$, third trace $\beta=-154.43^{o}\approx -144^{o}$ and finally the fourth trace $\beta=129.73-360^{o}=-230^{o}\approx -216^{o}$. The measured S-Parameter data were

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then imported to Ansys Designer for the combined simulation of the array, as shown in **Figure 4.34**

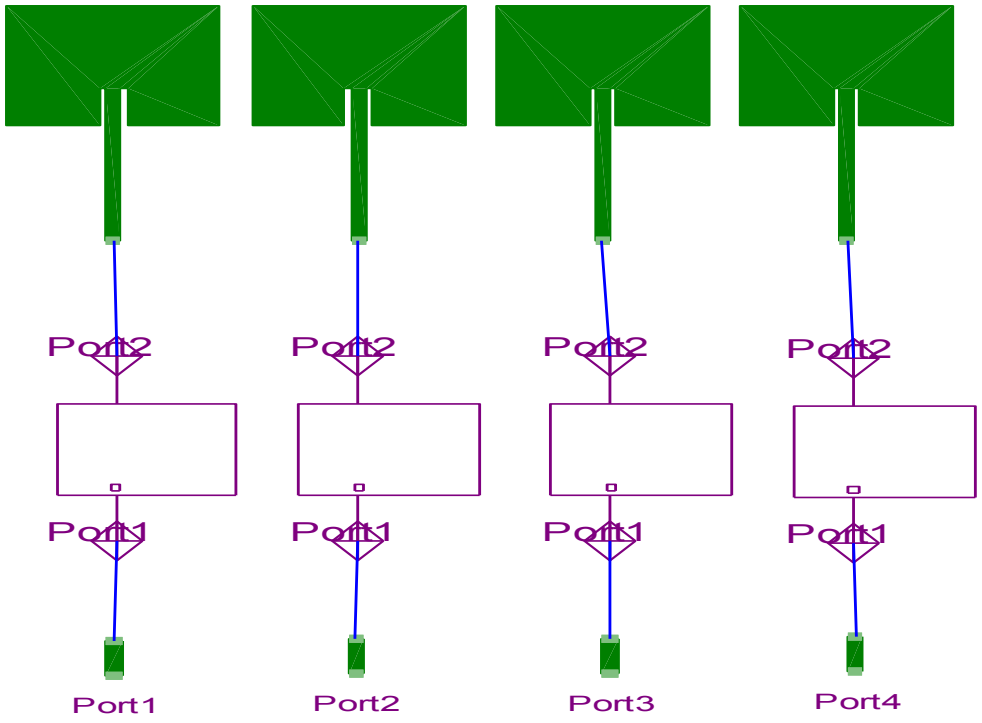

Figure 4.34 Importing the measured S-Parameters of the single stage phase shifter in Ansys Designer.

The simulated radiation patterns from Designer after incorporating the measured S-parameters are shown in **Figure 4.35** and **Figure 4.36.**

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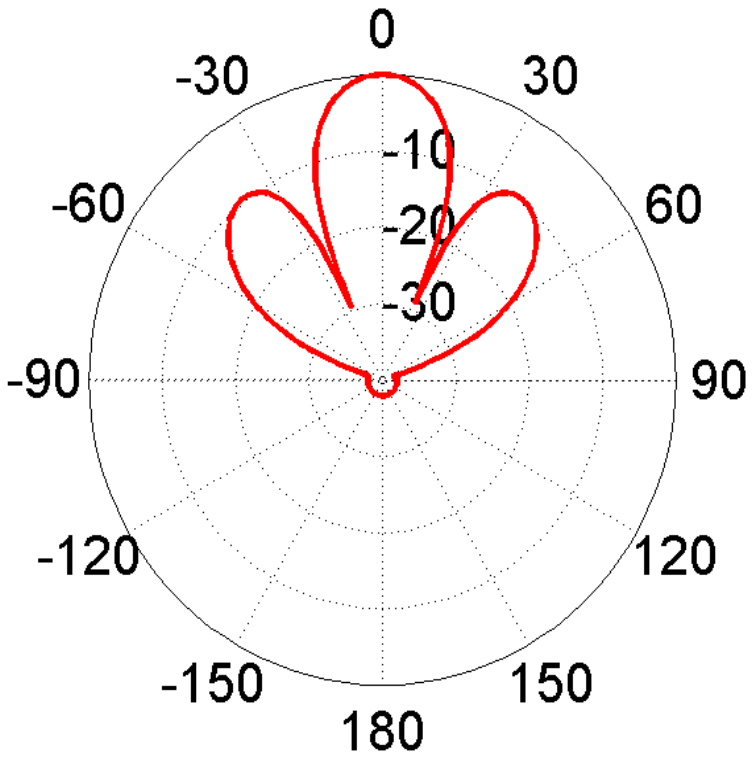

Figure 4.35 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=0 degree. Peak gain=10.8 dBi

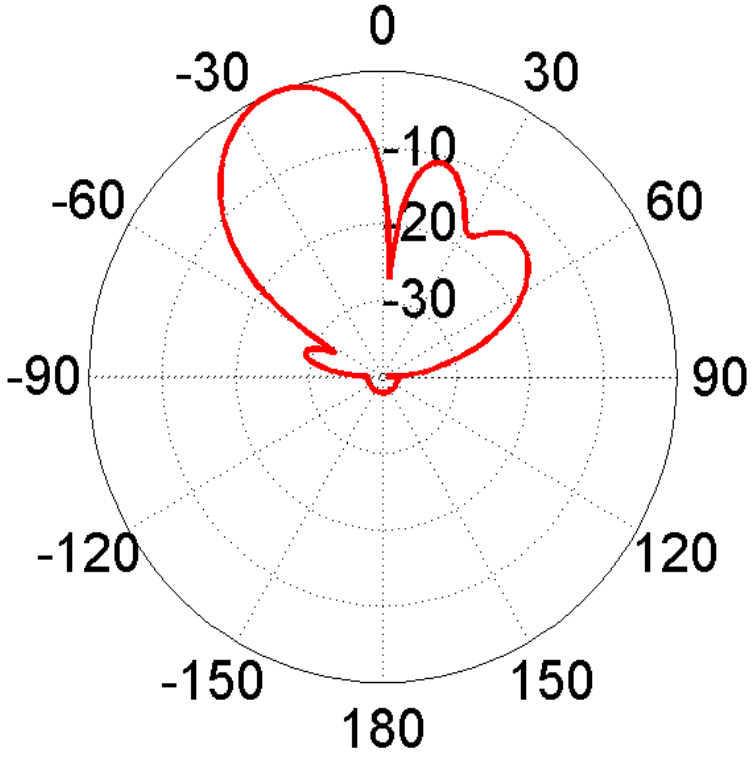

Figure 4.36 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-20 degree. Peak gain=9.9 dBi.

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4.6 Delay Lines Prototype Fabrication and Tests.

The delay lines were fabricated and populated with the previously mentioned GaAs SPDT switches. The delay lines were fabricated on 1.55 mm thick Duroid 5880 substrates. A photograph of the prototype delay lines is shown in **Figure 4.37.**

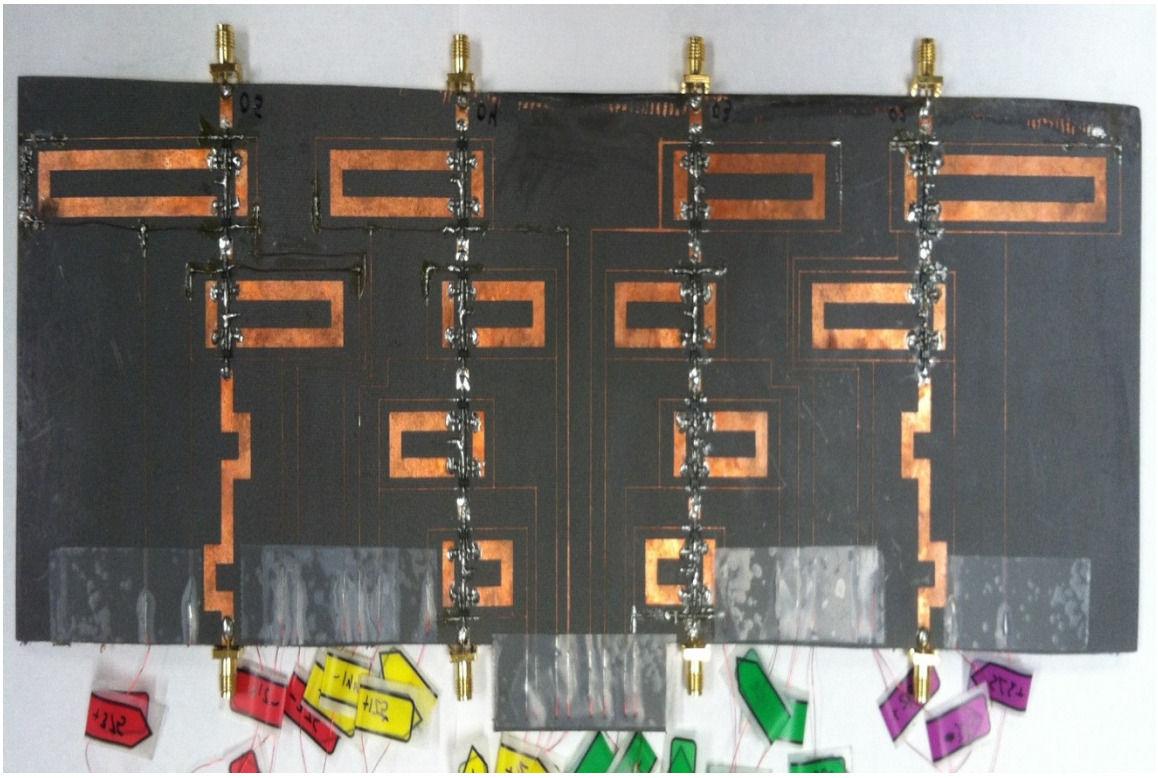

Figure 4.37 Photographs of fabricated delay lines containing GaAs SPDT switches.

The prototype of the delay lines required a total of 24 GaAs SPDT switches. An Agilent Vector Network Analyzer (VNA) was used to take the S-parameter measurements that

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reflected the insertion loss, return loss, and the phase delay. The measured S-Parameter data were then imported to Ansys Designer for combined simulation of the array, as shown in **Figure 4.38.**

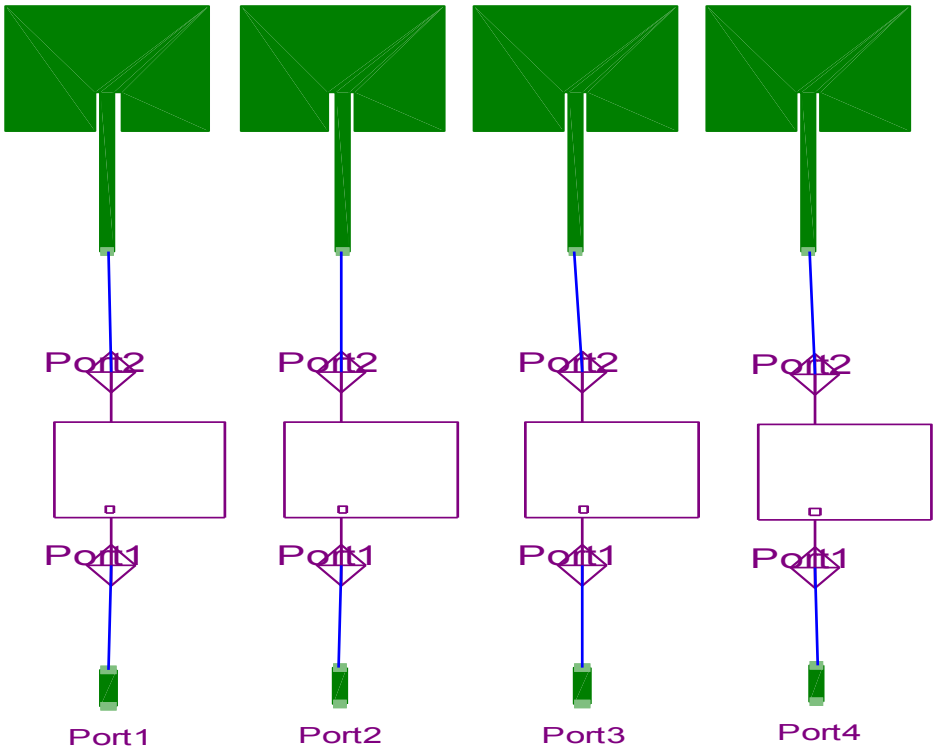

Figure 4.38 Importing the measured S-Parameters of the delay lines in Ansys Designer to feed the individual patches of the array.

The simulated radiation patterns from Designer after incorporating the measured S-parameters are shown in **Figure 4.39** to **Figure 4.43.**

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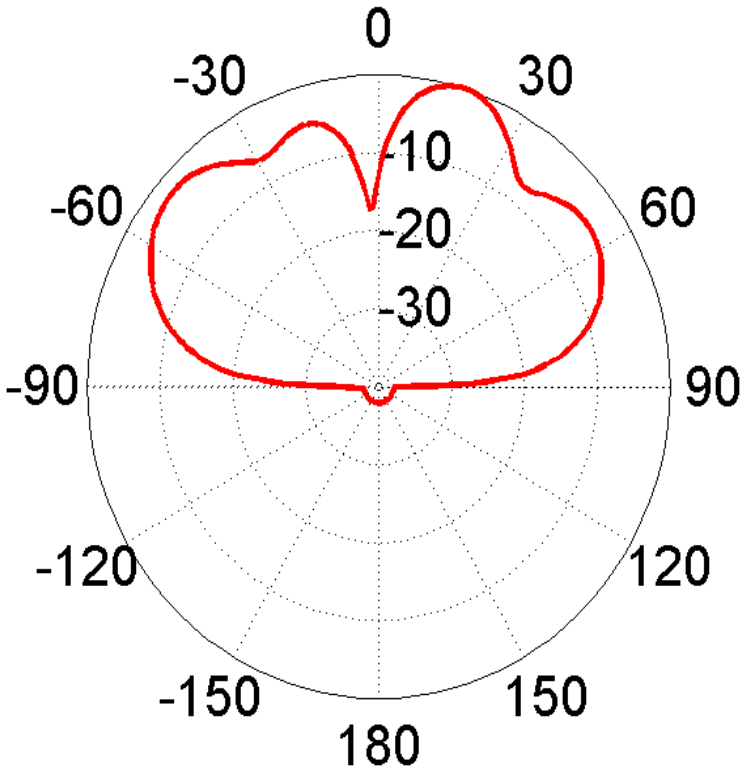

Figure 4.39 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-20 degree. Peak gain=-2.1 dBi.

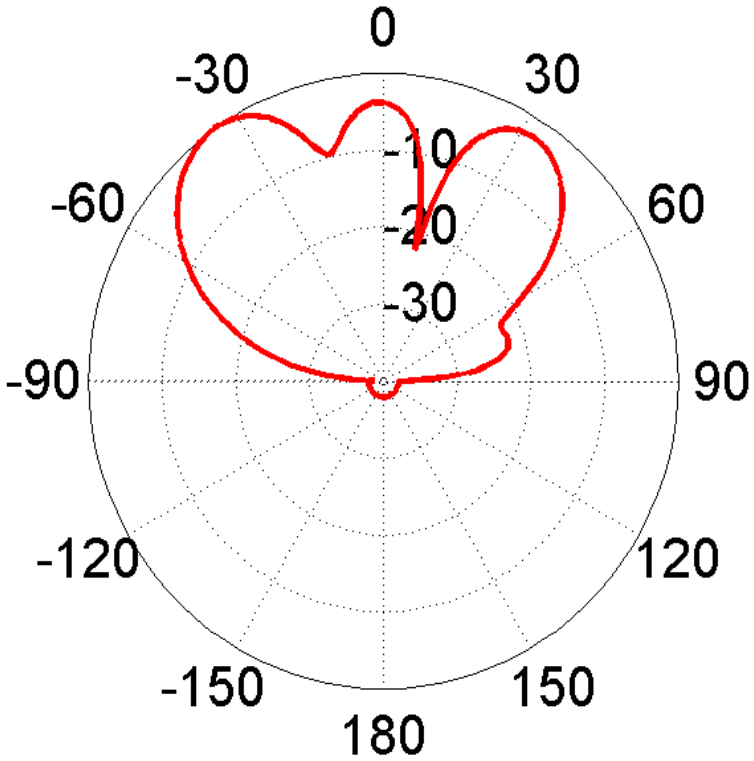

Figure 4.40 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-35 degree. Peak gain=4.1 dBi.

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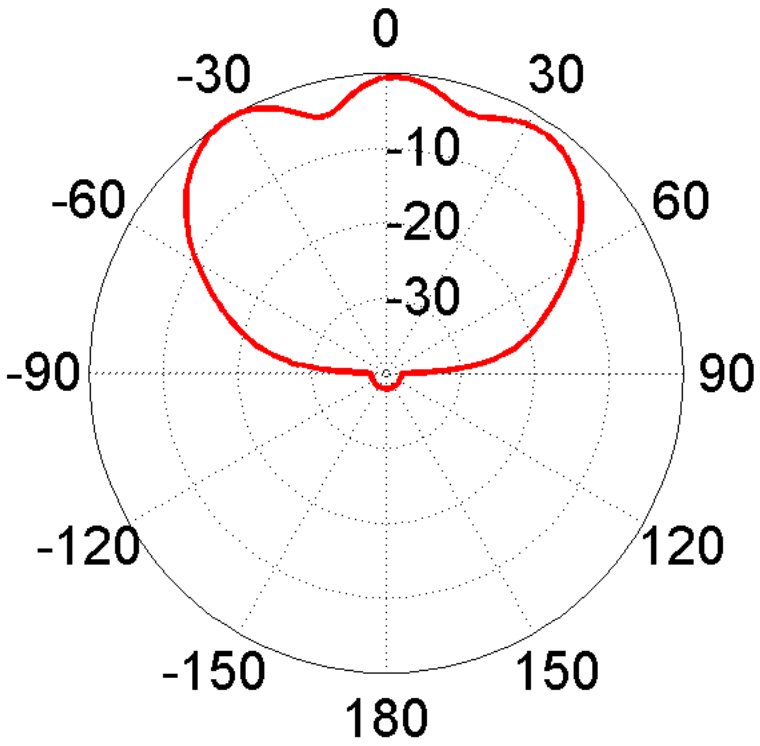

Figure 4.41 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=0 degree. Peak gain=2.7 dBi.

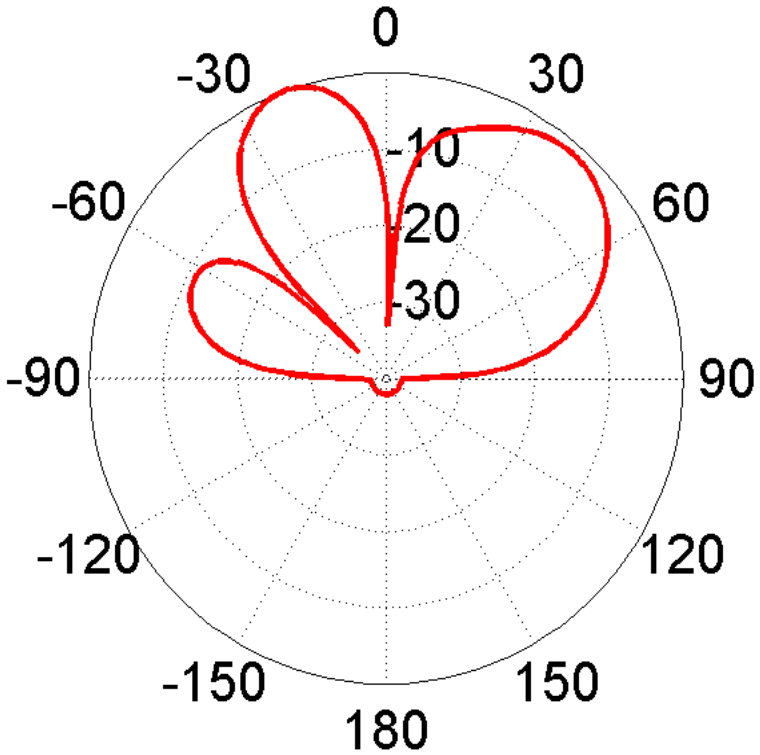

Figure 4.42 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=20 degree. Peak gain=-1.6 dBi.

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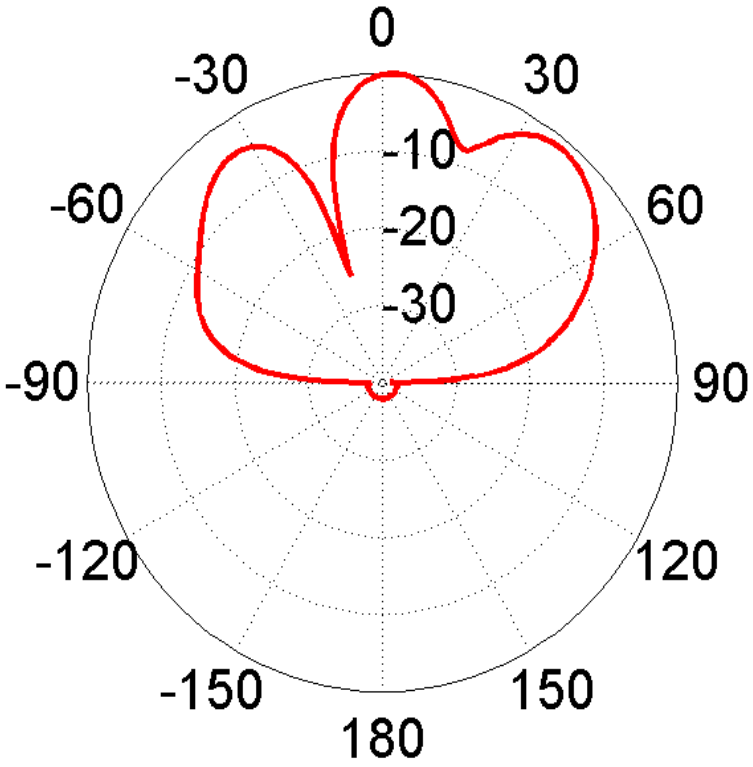

Figure 4.43 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=35 degree. Peak gain=3.4 dBi.

It is clear that the radiation patterns do not meet the expectations. The main beams are not well defined, beams are broad, and there are significant side lobes. After careful observation, it was found that there were phase errors in the design due to the asymmetry in the number of the switches in the delay lines because of the capacitors required to implement the switching circuits. The phase errors occurred because ports one and four had four switches while ports two and three had eight SPDT switches each. The extra four switches each in ports two and three

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were adding additional capacitances which needed to be compensated. The four extra SPDT switches at ports two and three are shown in **Figure 4.44**.

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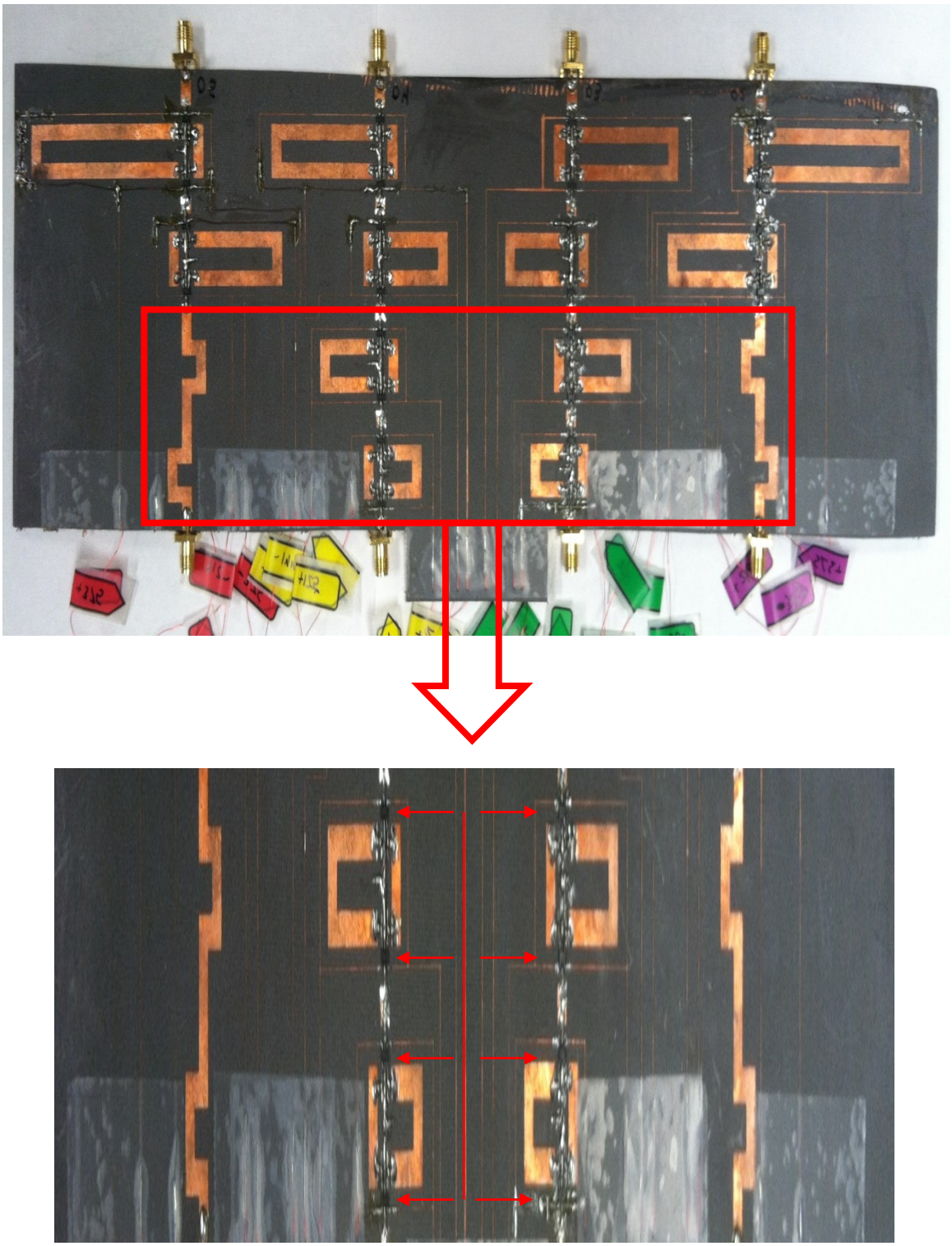

Figure 4.44 Close-up image of the prototype to show the extra four switches on ports two and three.

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To overcome this phase error additional delays at ports one and four were added. The modified design with the extra delay lines is shown in **Figure 4.45.**

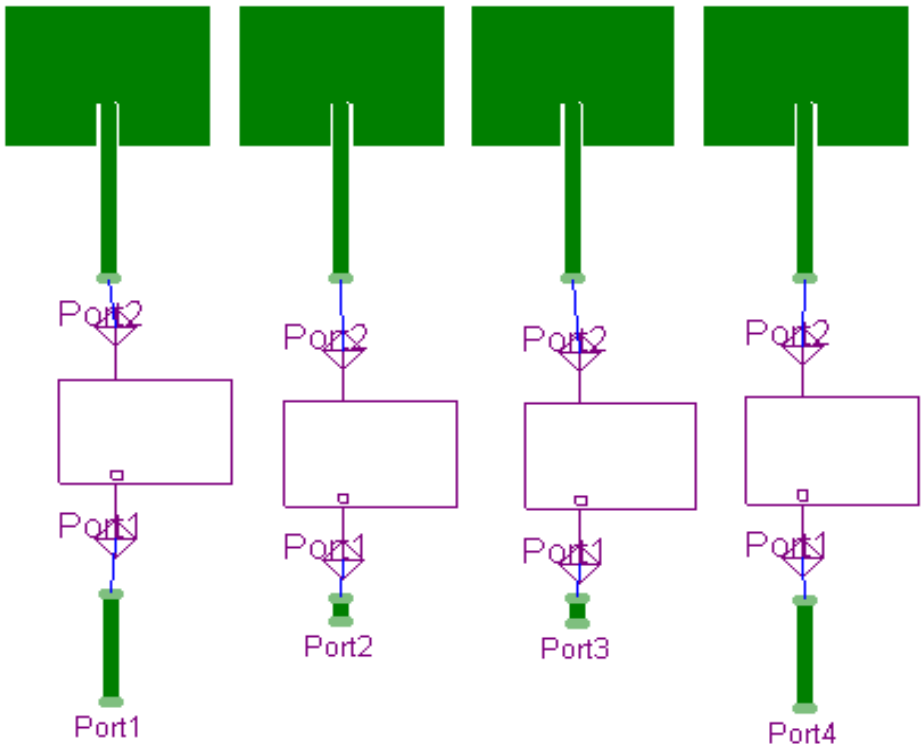

Figure 4.45 Modified design of the patch phased array in Ansys Designer.

After the phase error compensation simulations were run again, the results of which are shown in **Figure 4.46** to **Figure 4.50.**

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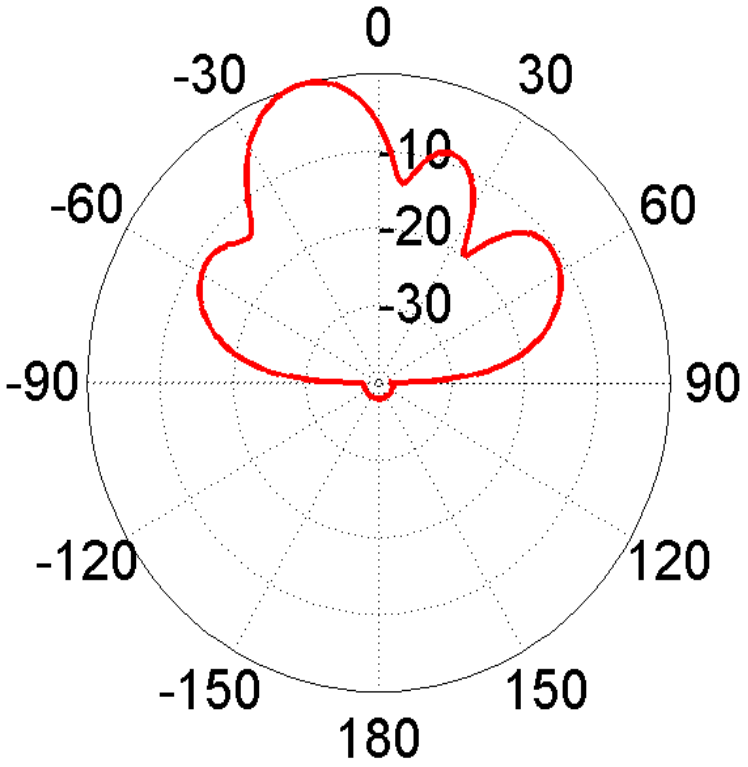

Figure 4.46 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-20 degree. Peak gain=7.4 dBi.

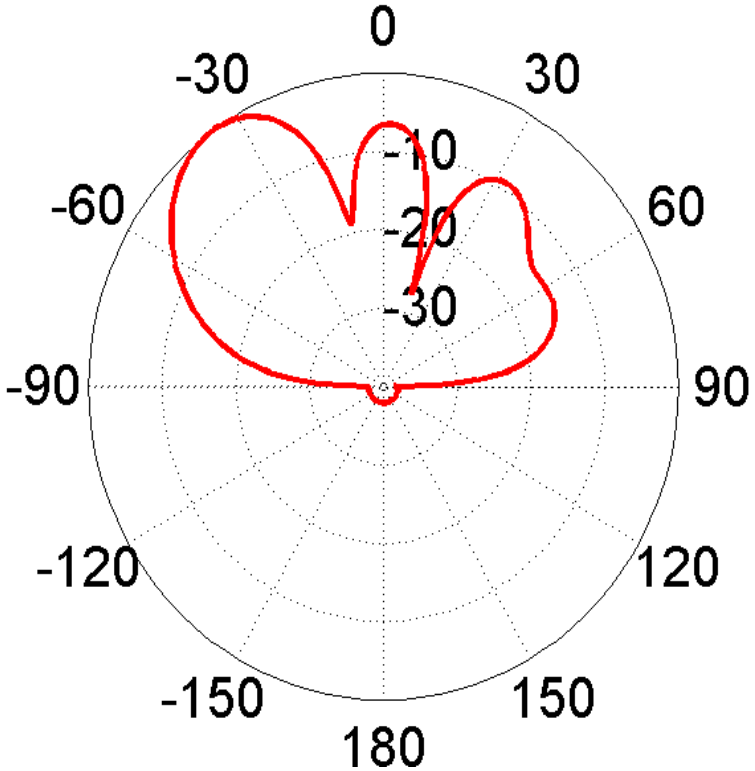

Figure 4.47 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-35 degree. Peak gain=7.4 dBi.

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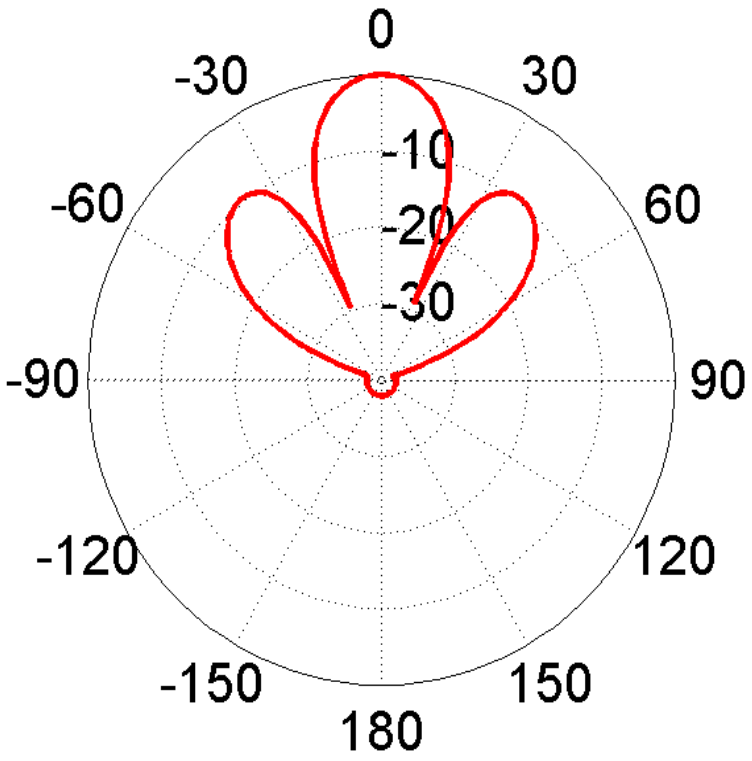

Figure 4.48 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=0 degree. Peak gain=8.1 dBi.

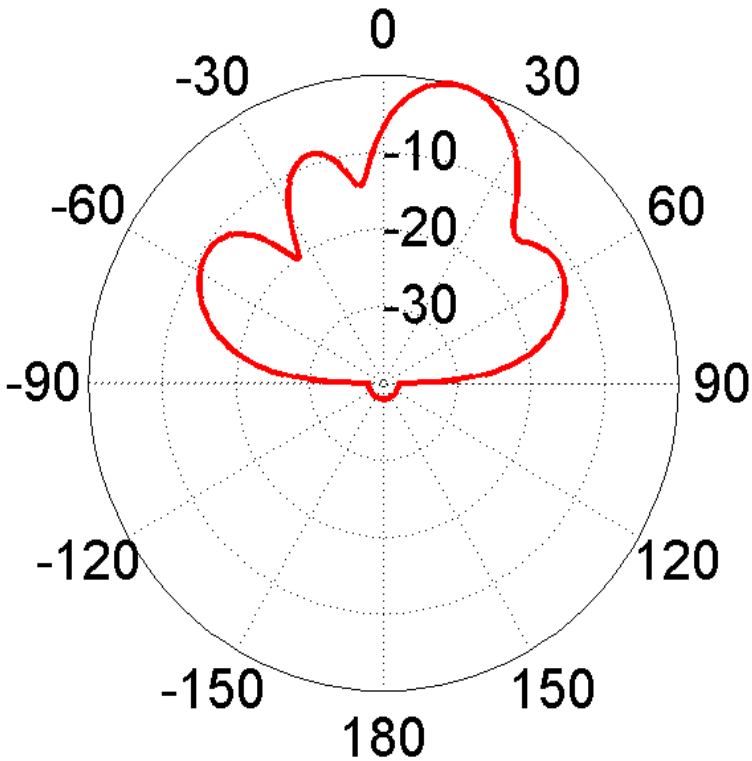

Figure 4.49 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=20 degree. Peak gain=7.4 dBi.

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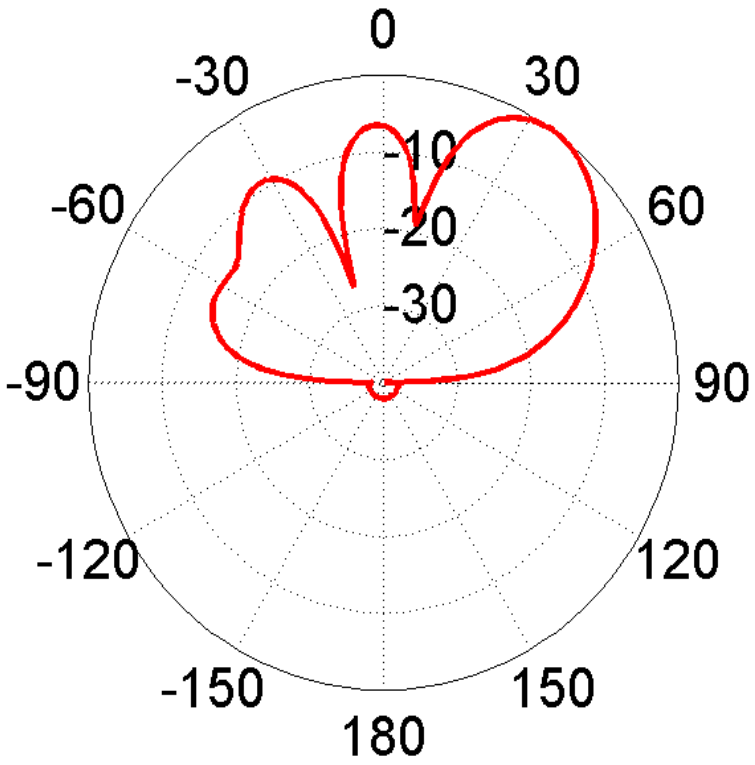

Figure 4.50 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=35 degree. Peak gain=7.4 dBi.

These radiation patterns in general meet our design goals. Note that each pattern simulated in Designer does not show any radiation in the lower hemisphere because Designer considers an infinite ground plane and hence restricts the radiation below.

After that we used the Dynamic Link feature between HFSS and Ansys Designer to push the S-Parameters measurements data that were incorporated into Designer into HFSS as shown in **Figure 4.51**. The radiation patterns obtained from HFSS are shown in **Figure 4.52** to **Figure 4.56**.

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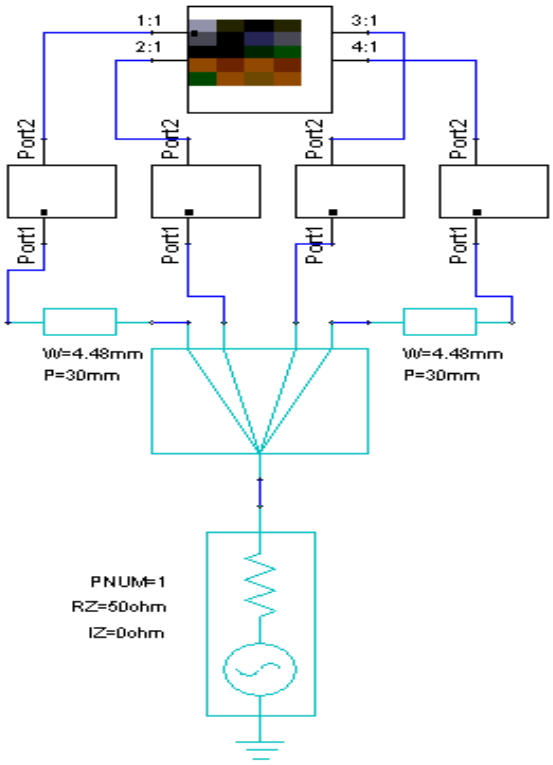

Figure 4.51 Pushing the excitations into HFSS through Dynamic Link.

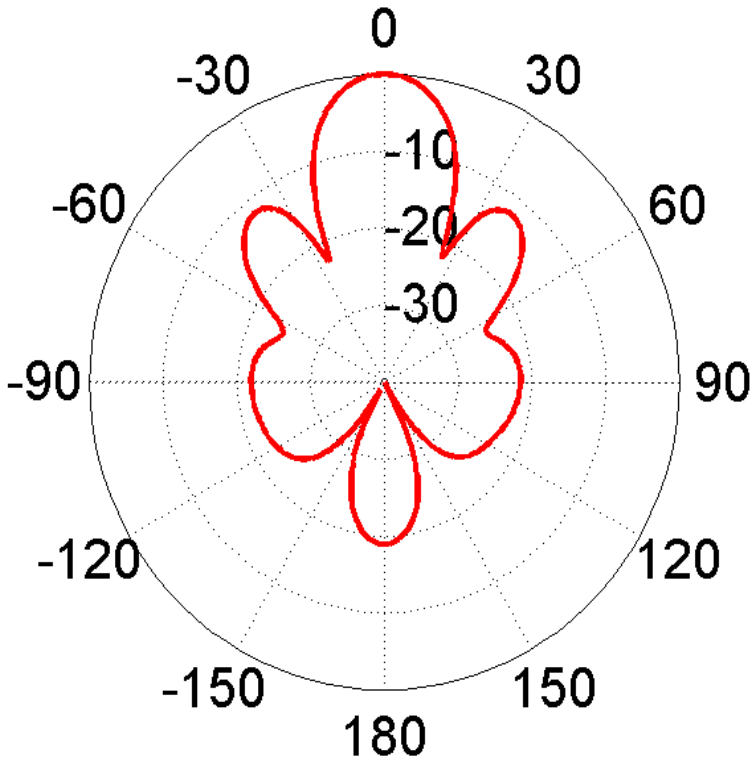

Figure 4.52 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=0 degree.

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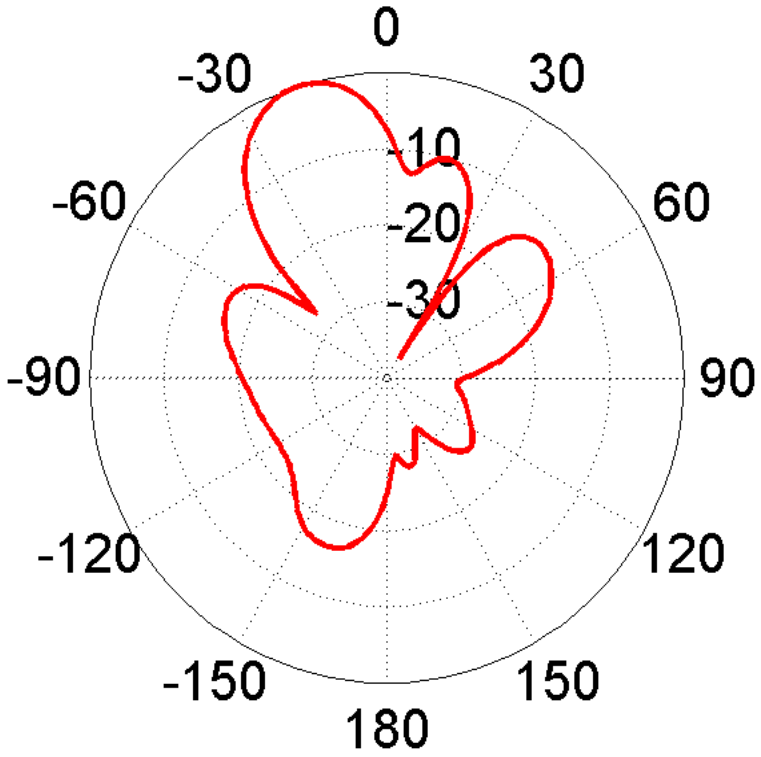

Figure 4.53 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-20 degree.

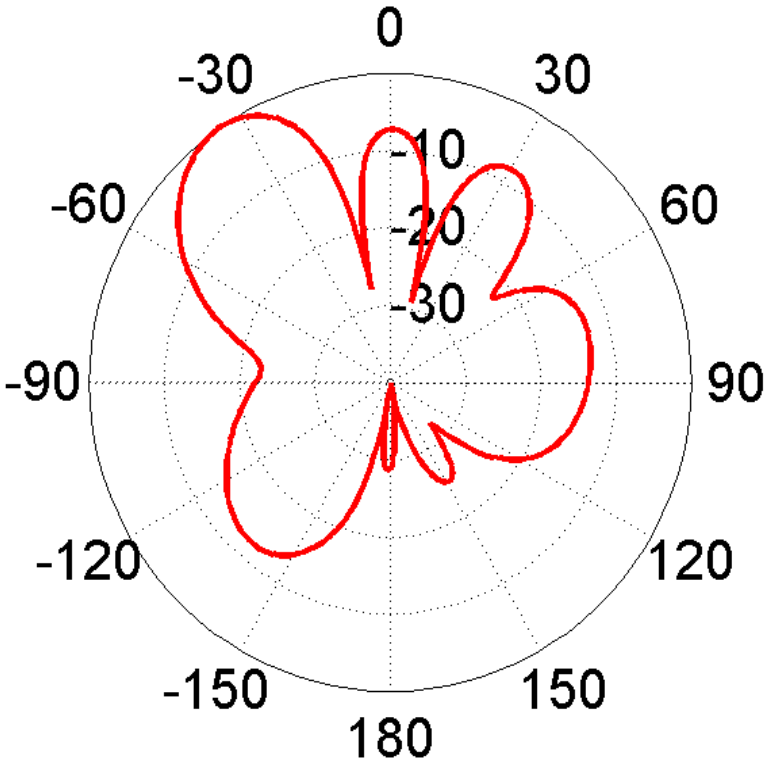

Figure 4.54 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=-35 degree.

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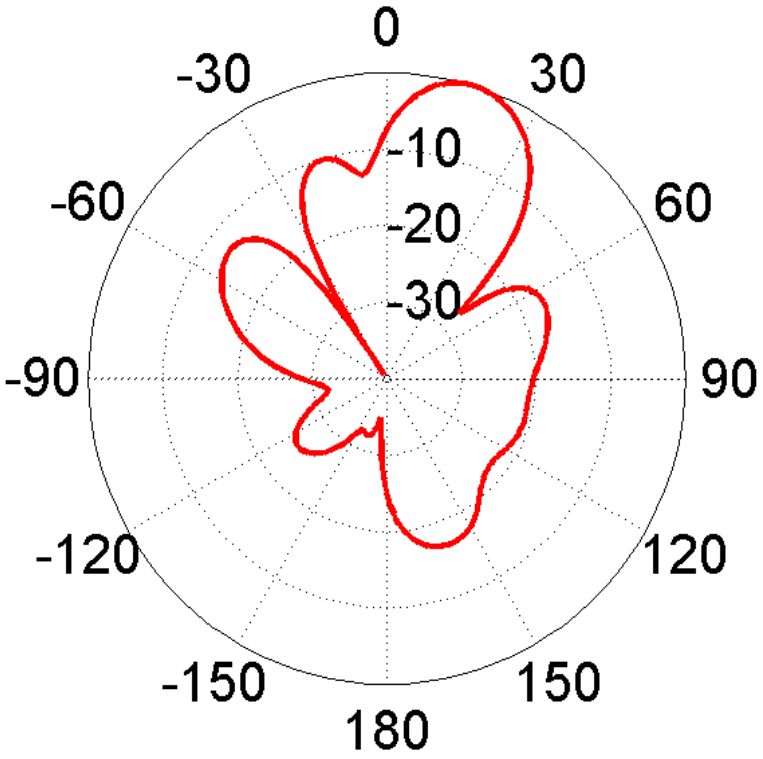

Figure 4.55 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=20 degree.

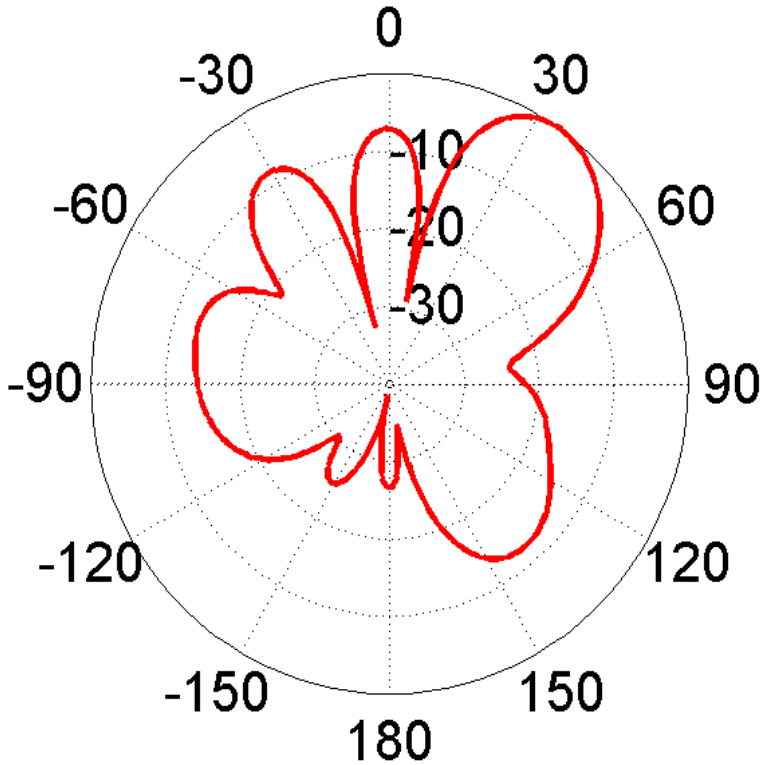

Figure 4.56 Radiation pattern of the patch array with the beam peak directed along $\boldsymbol{\theta_0}$=35 degree.

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We could see that the radiation patterns do match the design goals when using the Dynamic Link between HFSS and Designer.

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CHAPTER 5

PROPOSED PHASED ARRAY CPW-FED SLOT ANTENNA

5.1 Single Element Slot Antenna

The radiating element that is used in this design is a broadband semicircular coplanar waveguide-fed slot antenna. Slot antennas are widely used in applications that require planar low-profile antennas. Slots eliminate the need for via holes and reduce radiation losses. Shown in **Figure 5.1** is a novel design of a broadband semicircular slot antenna[10].

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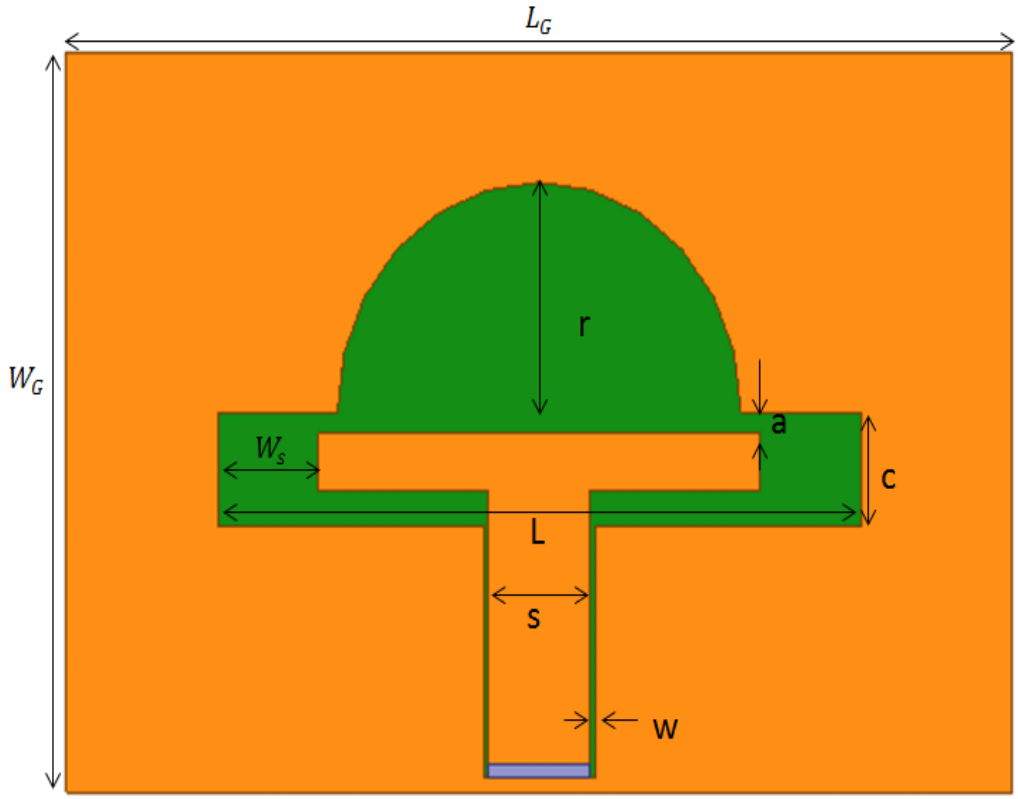

Figure 5.1 Designed novel semicircular slot antenna[5].

The slot antenna shown in **Figure 5.1**, is designed on Duroid 5880 substrate ($\varepsilon_r = 2.2$) with length L_G=75 mm, width W_G= 51 mm. Other parameters are: radius, r= 16 mm, c= 8 mm, a=1.5 mm, W_S= 8 mm, L= 51 mm, s= 8 mm and w= 0.4 mm to have the optimum results.

The proposed slot antenna was modeled and simulated using Ansys HFSS. Simulated $|S_{11}|$ (dB) data are shown in **Figure 5.2**. It is clear that the operating frequency of the slot antenna extends from approximately 2 GHz to 5.5 GHz.

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Shown in **Figure 5.3** is the VSWR which shows that the VSWR is below 2 starting from 2 GHz to 5.5 GHz.

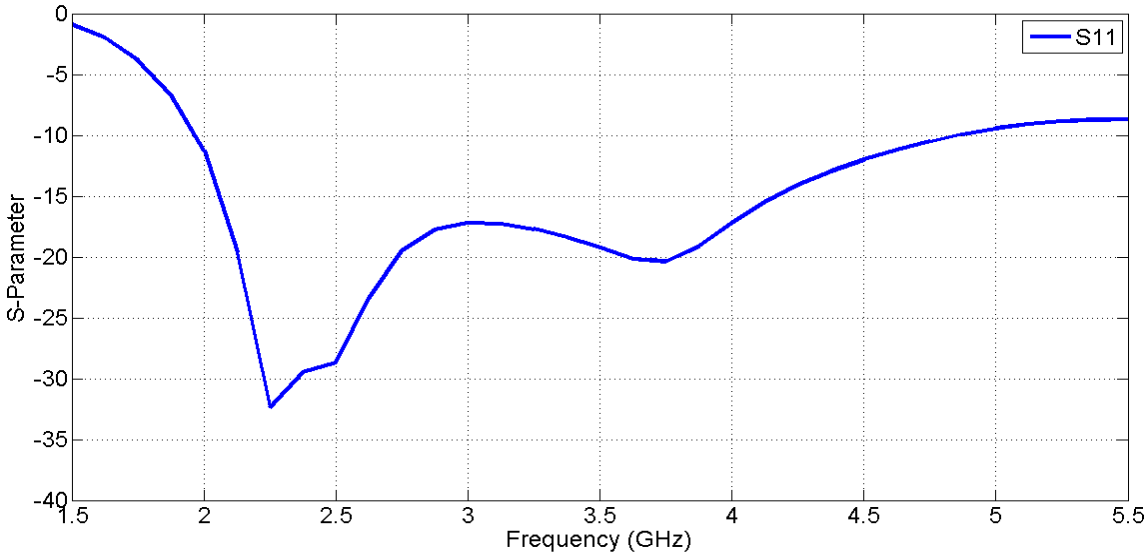

Figure 5.2 Simulated $|S_{11}|$ data of the semicircular slot antenna in dB.

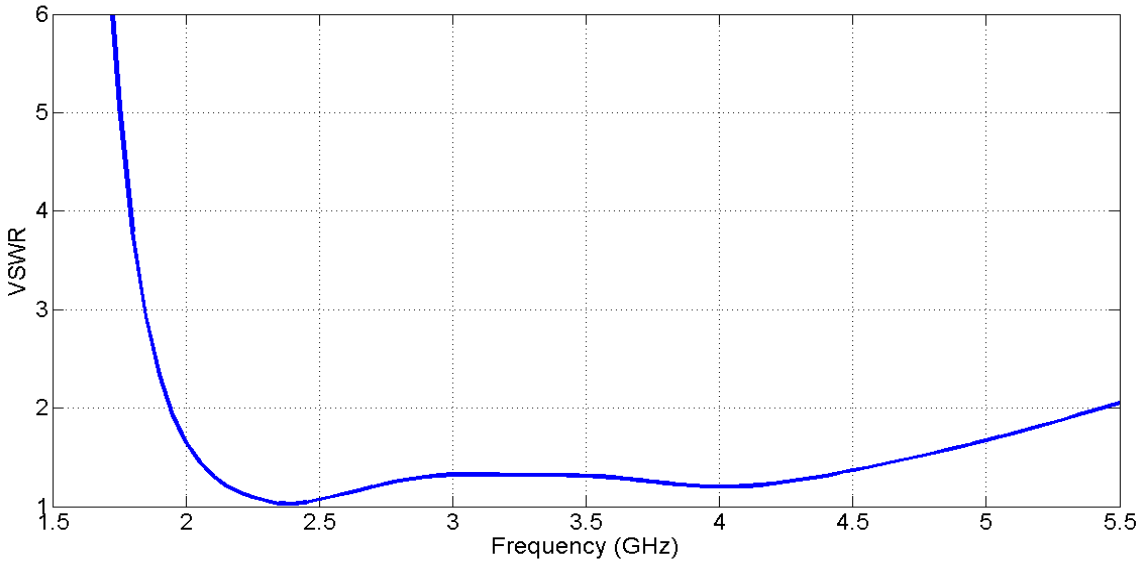

Figure 5.3 Simulated VSWR of the single element semicircular slot antenna on Duroid 5880.

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Radiation patterns in both the E and H planes are shown in **Figure 5.4**

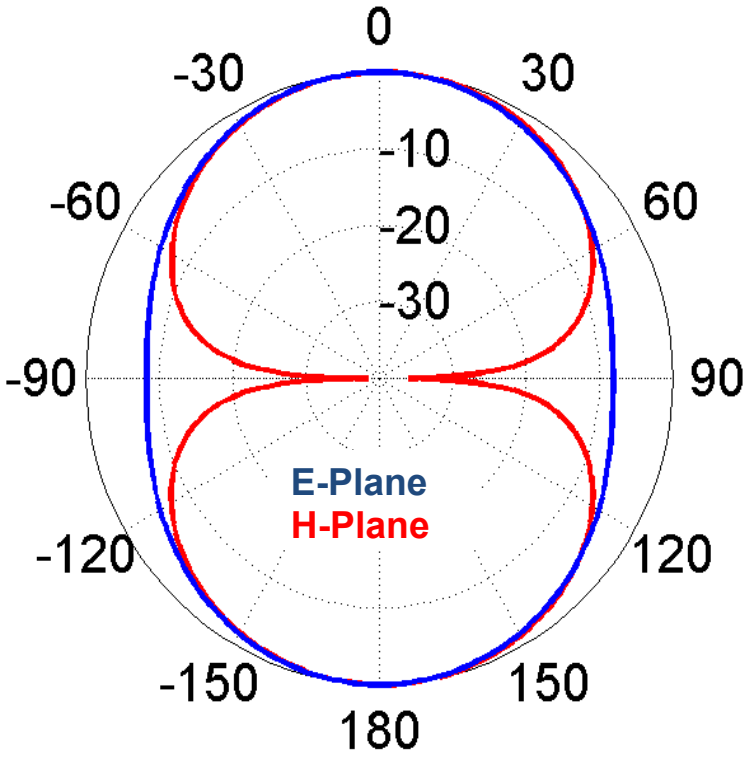

Figure 5.4 Simulated radiation patterns of the semicircular slot antenna on Duroid 5880. Peak gain=4.5 dBi.

The semicircular slot antenna radiates in both directions meaning both the upper and lower sides of the substrate.

5.2 Semicircular Slot Phased Array

A four element phased array consisting of the semicircular slot antenna was modeled and simulated using HFSS along a straight line making it a linear array. The array would increase the gain magnitude and would introduce the scanning behavior with broadband capability. The four

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element semicircular slot array designed and simulated using HFSS is shown in **Figure 5.5.**

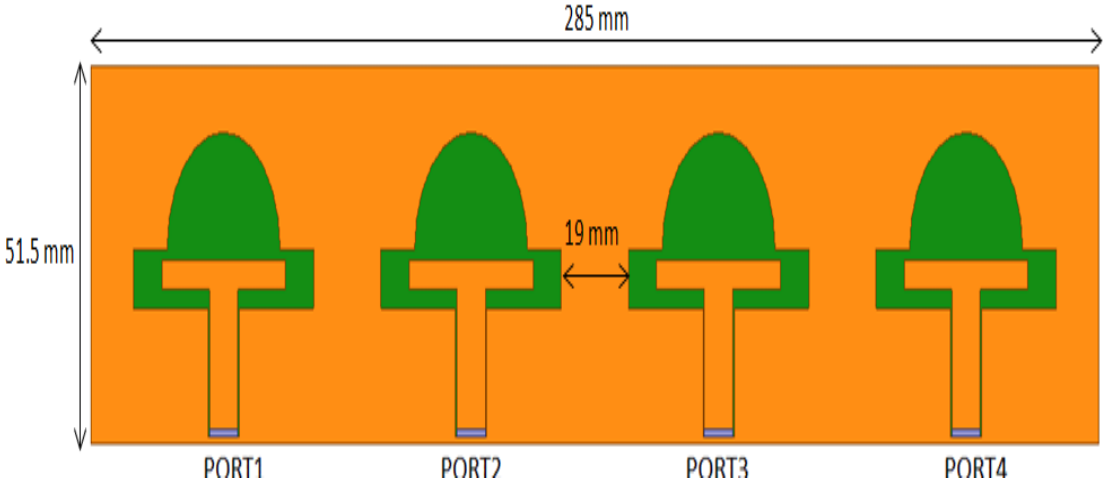

Figure 5.5 The four-element semicircular slots array modeled in HFSS.

Initially the slot array was simulated considering four separate feeds as shown in **Figure 5.5.** Simulated S-parameters of this slot array are shown in **Figure 5.6.**

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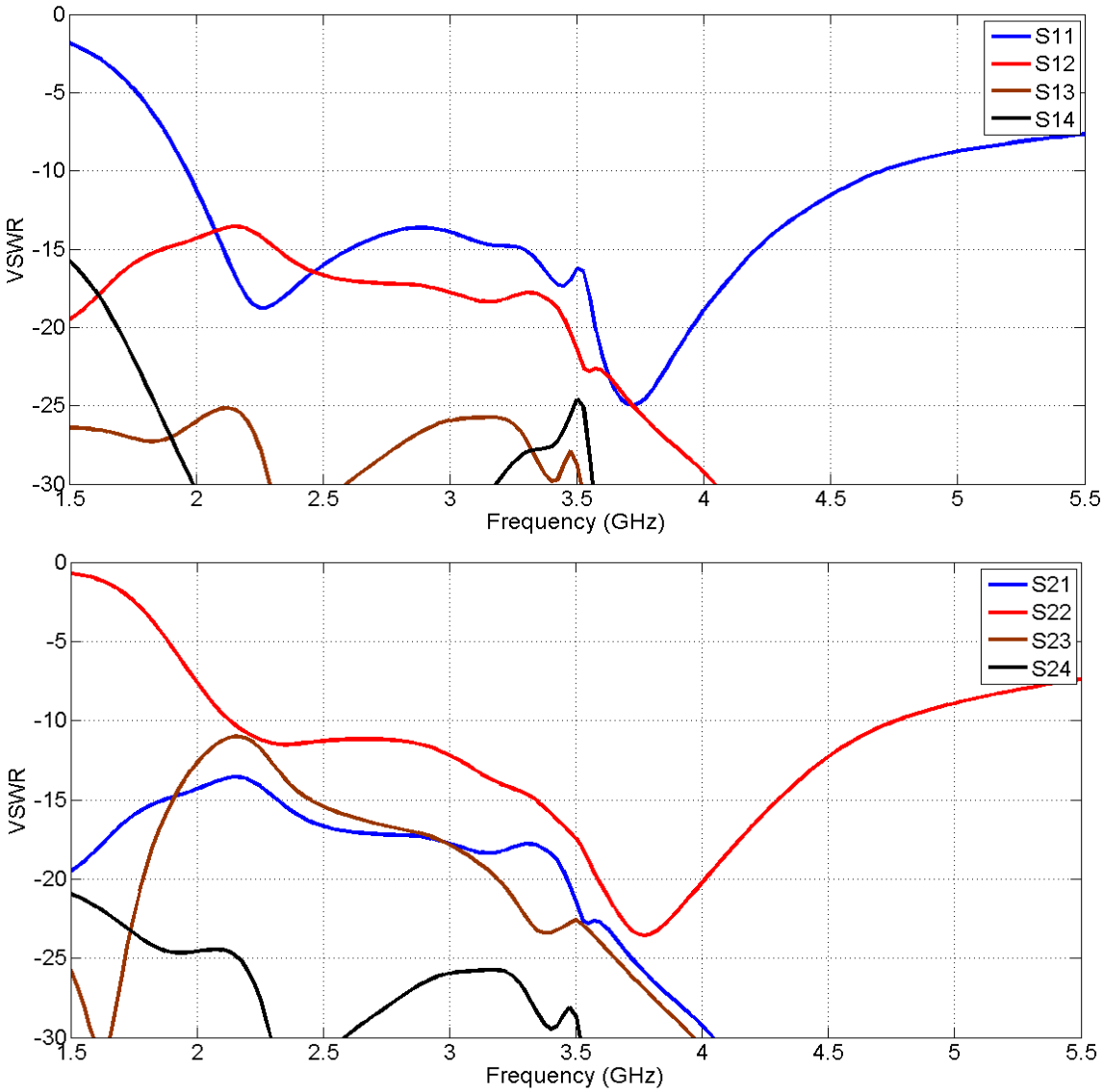

Figure 5.6 Simulated S-parameters of the semicircular slot array.

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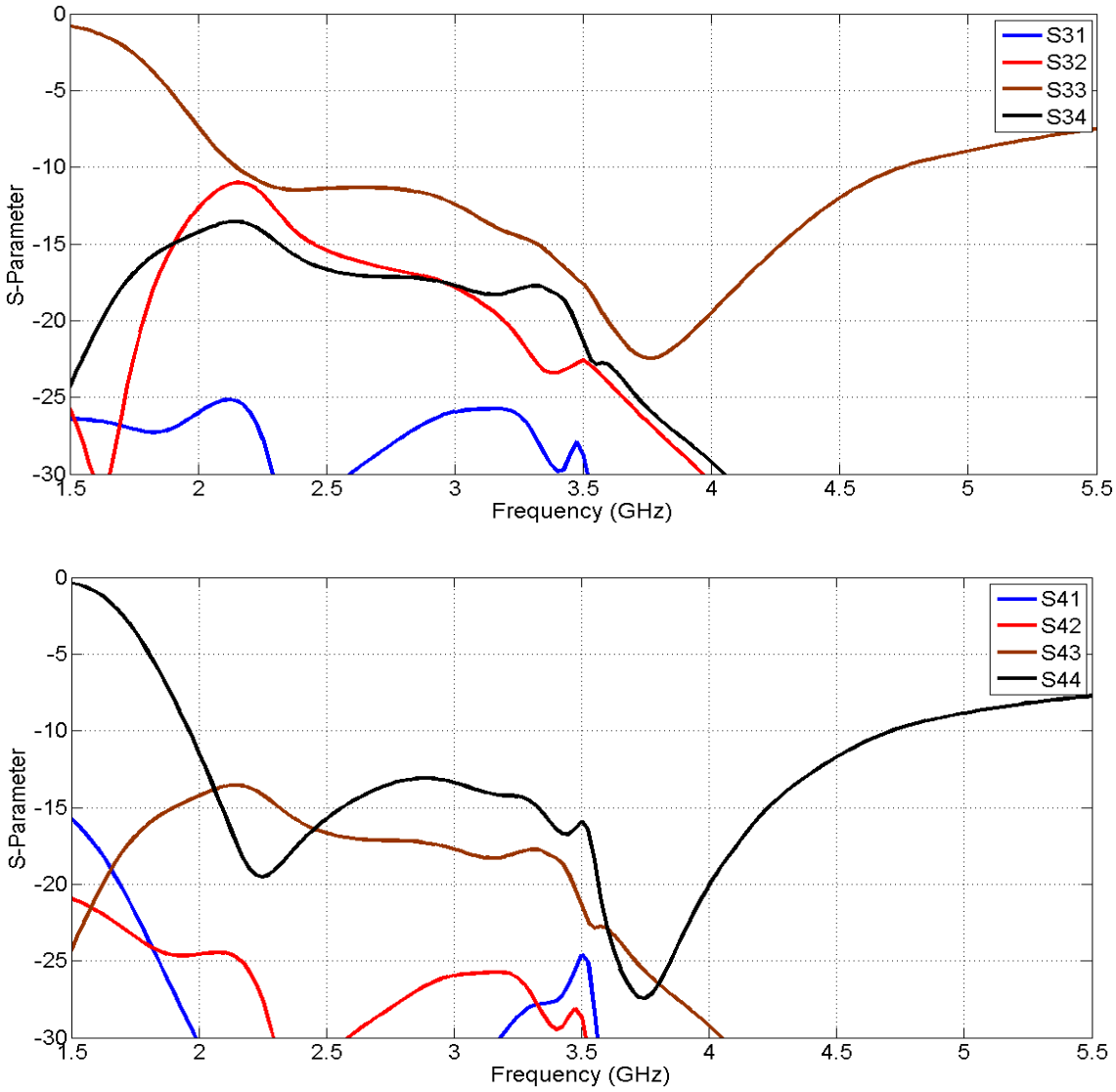

Figure 5.6 Simulated S-parameters of the semicircular slot array.

Complementary VSWR plot of the array is shown in **Figure 5.7.**

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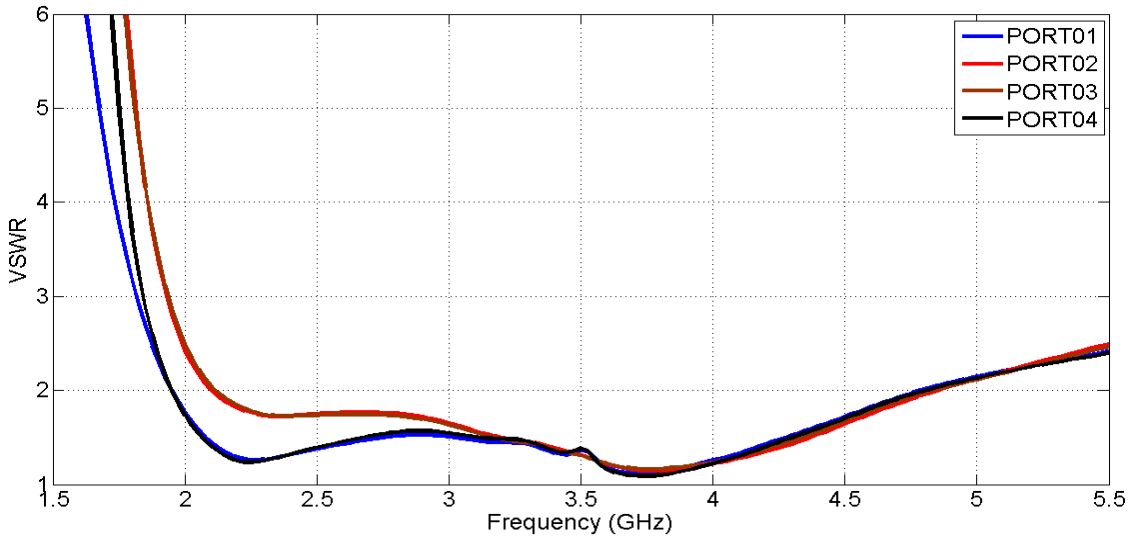

Figure 5.7 Simulated VSWR data of the semicircular slot array on Duroid 5880.

Comparing the radiation pattern of the array shown in **Figure 5.8** with that shown in **Figure 5.4,** it is obvious that the array has higher gain (9.6 dBi compared to 4.5 dBi).

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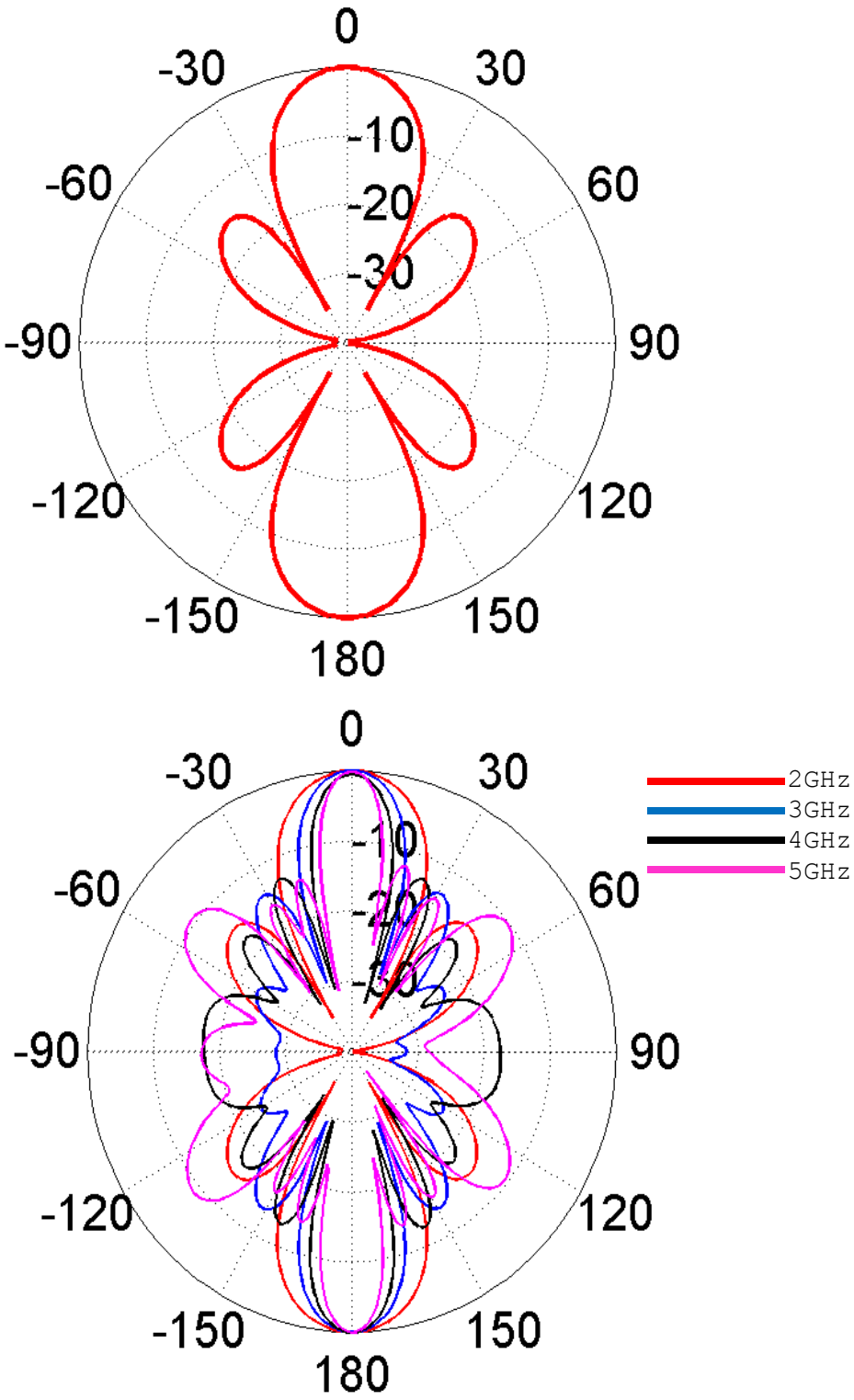

Figure 5.8 Radiation pattern of the semicircular slot antenna array with the beam at $\boldsymbol{\theta_0}$=0 degree. Peak gain=9.6 dBi.

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Then, simulations were performed to investigate the beam scanning behavior of the array. The progressive phase shift β of the feeding ports were changed according to **Figure 5.9** and **Table 4.2** to scan the beam as desired.

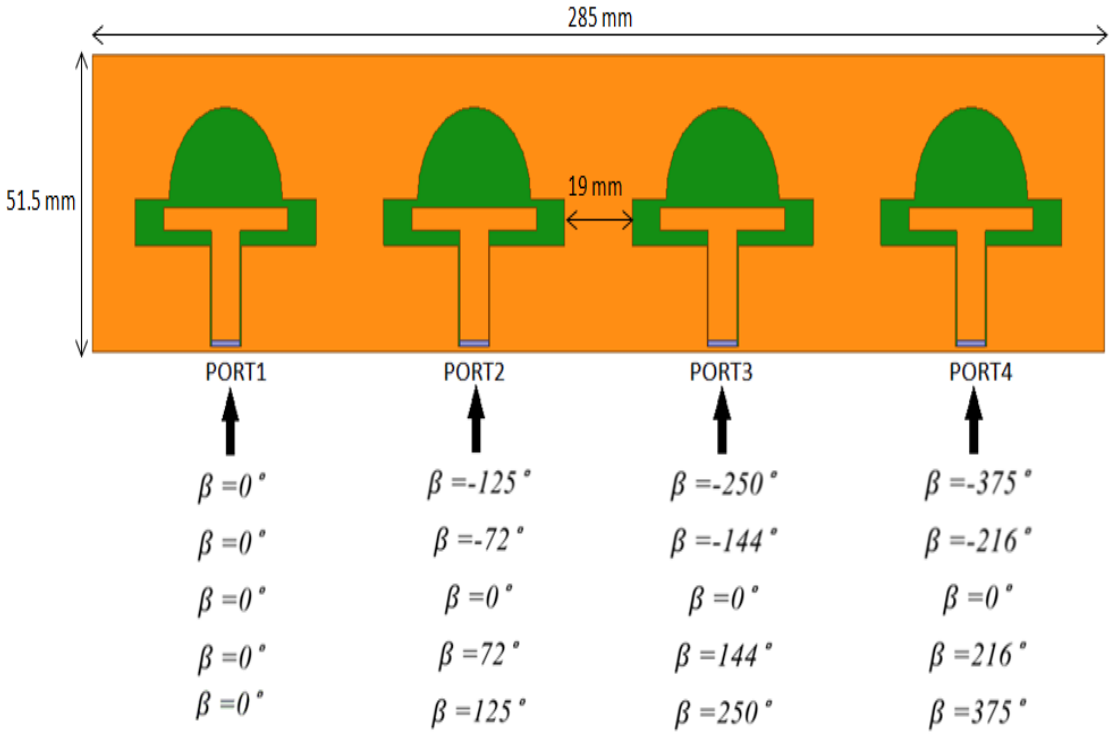

Figure 5.9 Progressive phase shift $\boldsymbol{\beta}$ required to scan the beam along the desired angles.

The radiation patterns for the semicircular slot antenna array for different values of the progressive shift are shown in **Figure 5.10** to **Figure 5.13**. Notice that the slot antenna array scans its beam in both directions, as expected.

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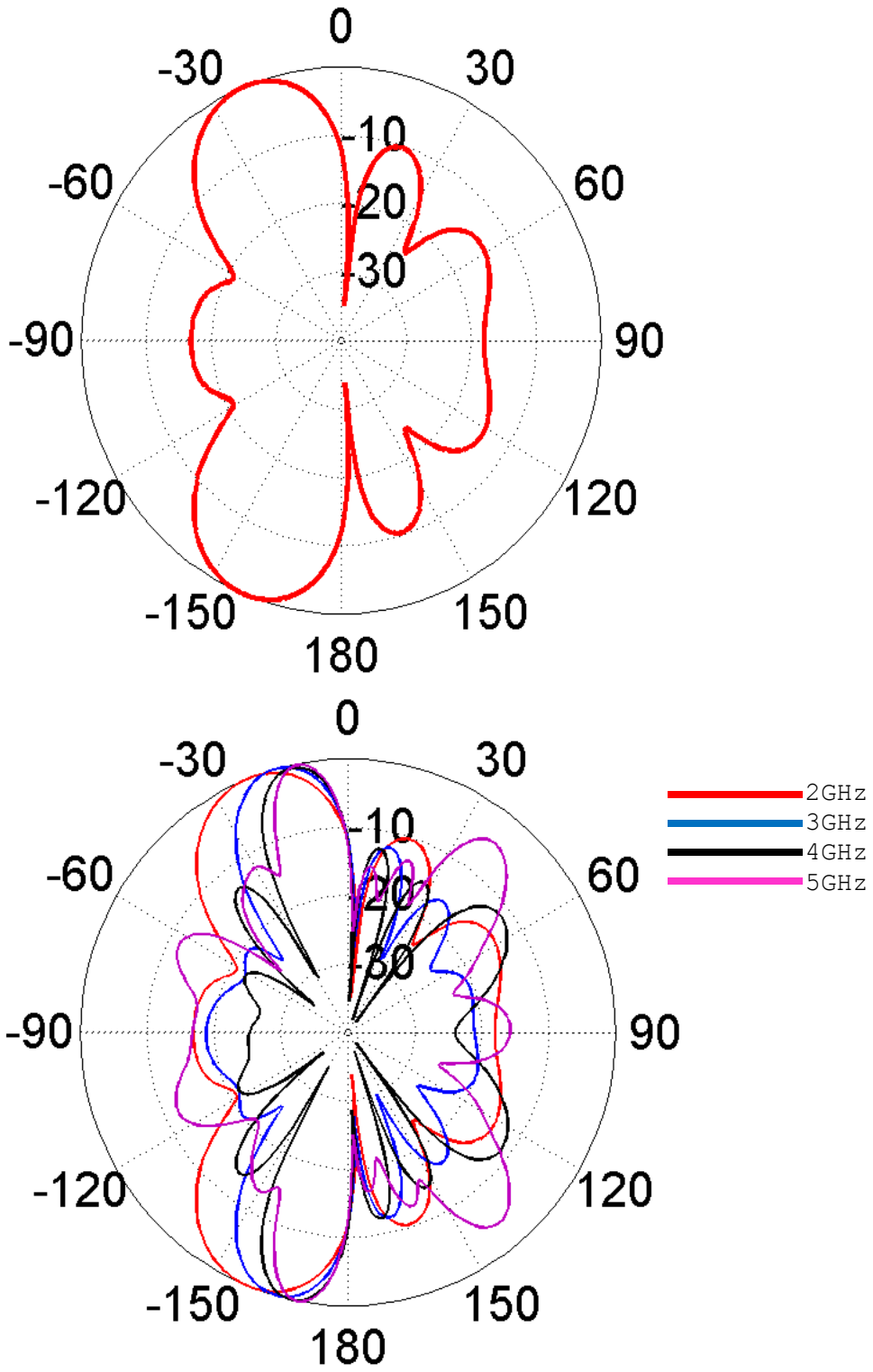

Figure 5.10 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=-20 degree. Peak gain=8.8 dBi.

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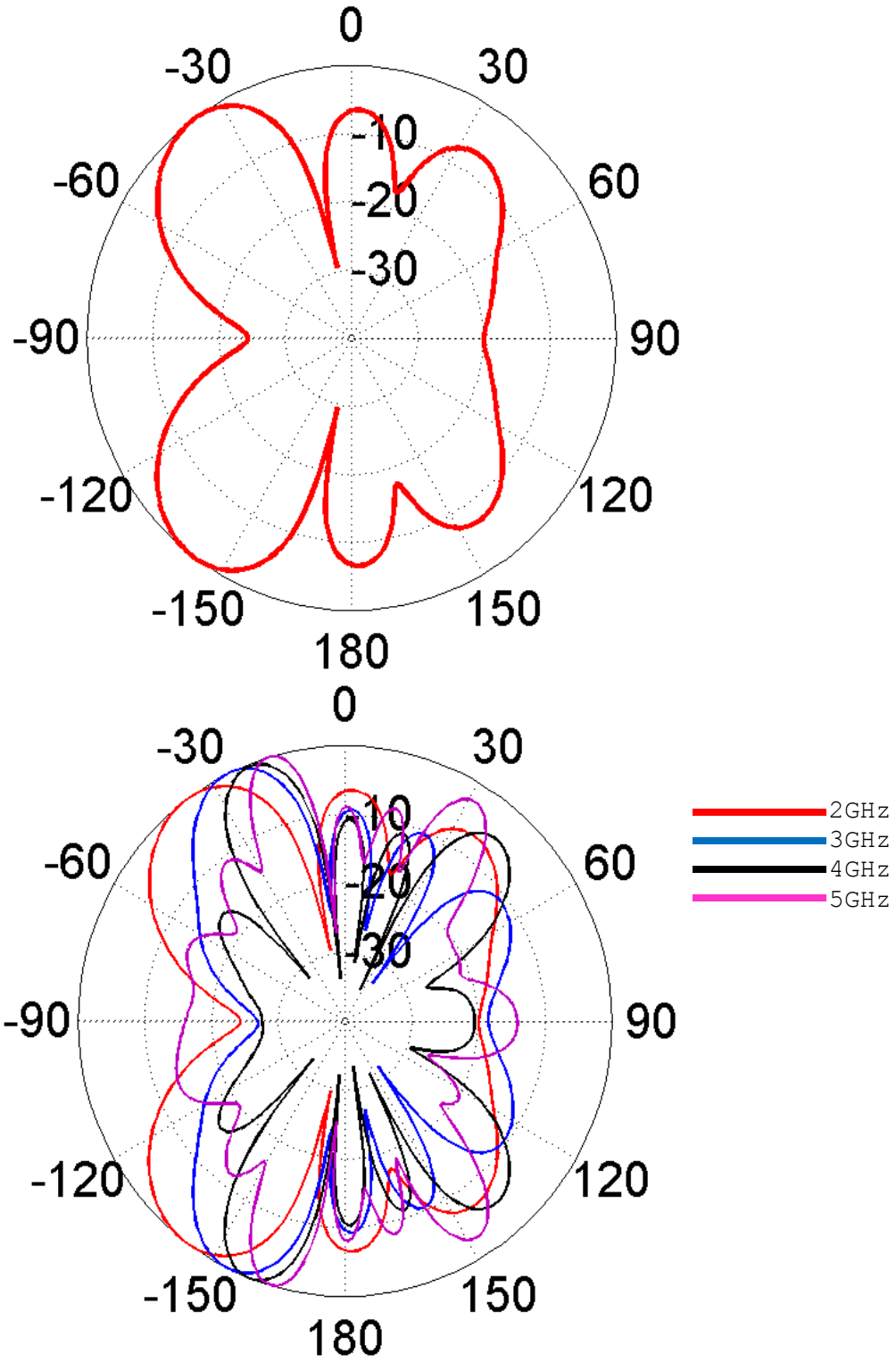

Figure 5.11 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=-35 degree. Peak gain=6.1 dBi.

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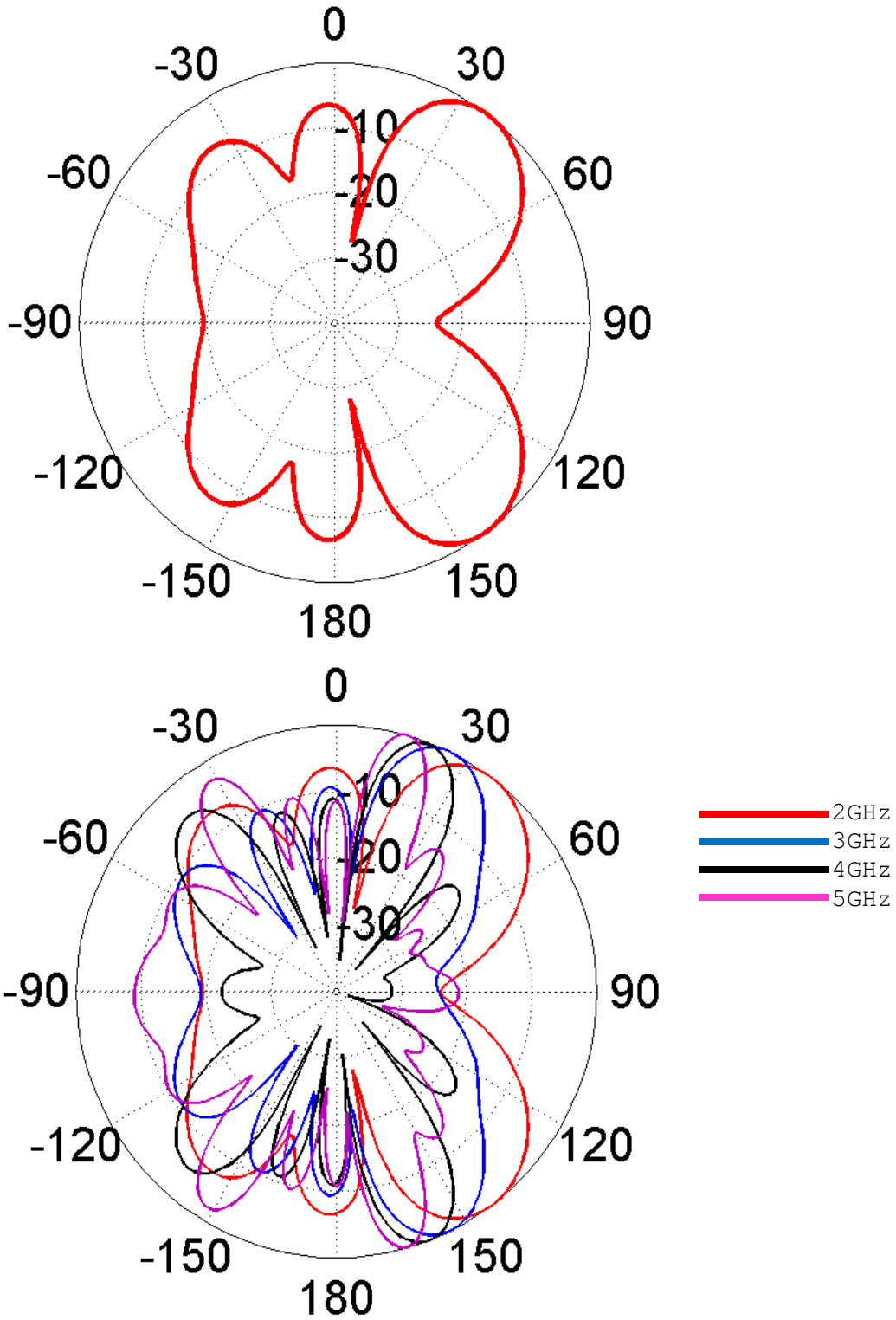

Figure 5.12 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=35 degree. Peak gain=6.1 dBi.

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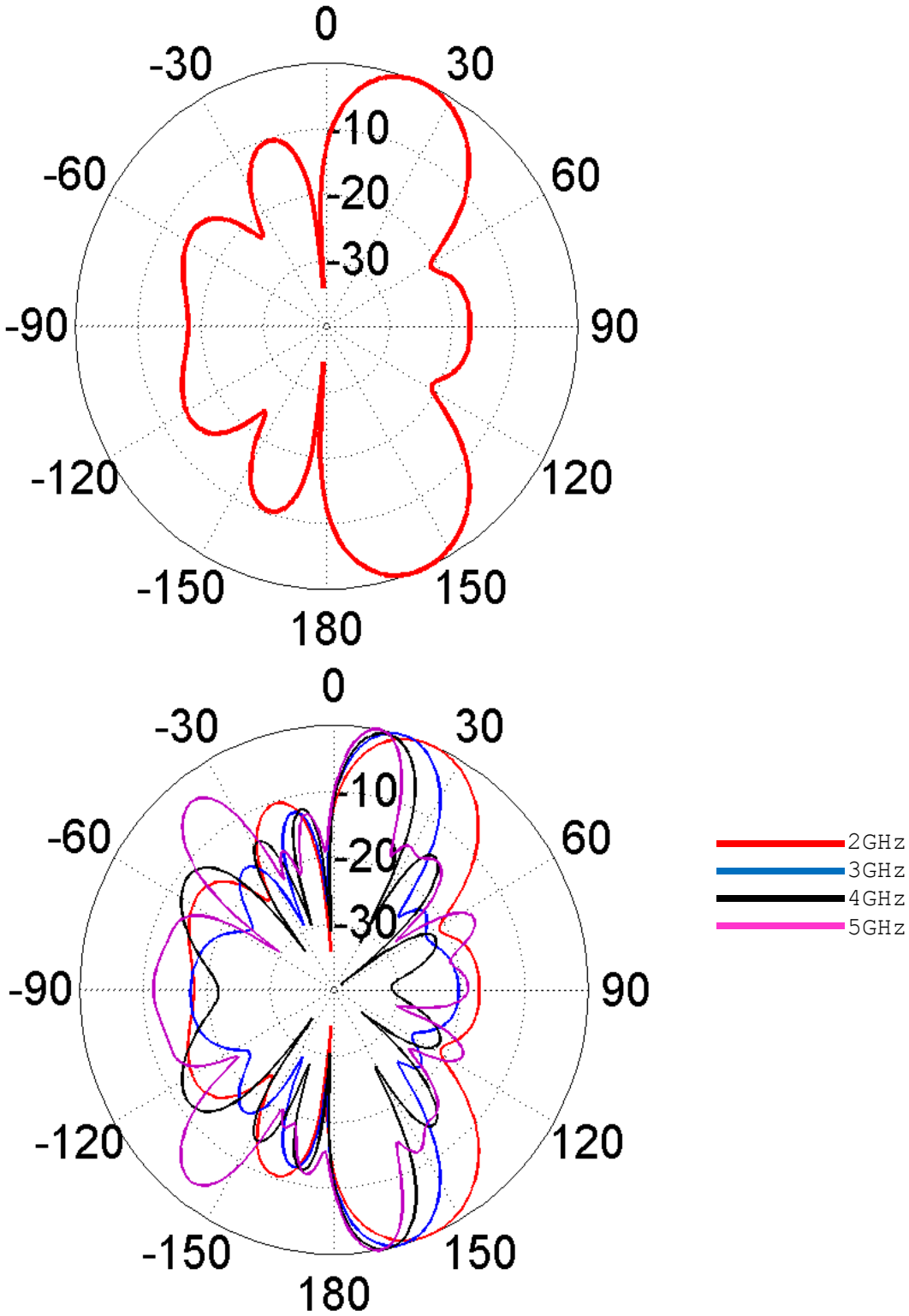

Figure 5.13 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=20 degree. Peak gain=8.8 dBi.

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Next, we used the Dynamic Link feature between HFSS and Ansys Designer to push the S-Parameters measurement data that were taken from the delay lines prototype. The measurements were incorporated into Designer to be pushed to the design that was modeled in HFSS as shown in **Figure 5.14.** The radiation patterns results obtained from HFSS are shown in Figure 5.15 to Figure 5.19.

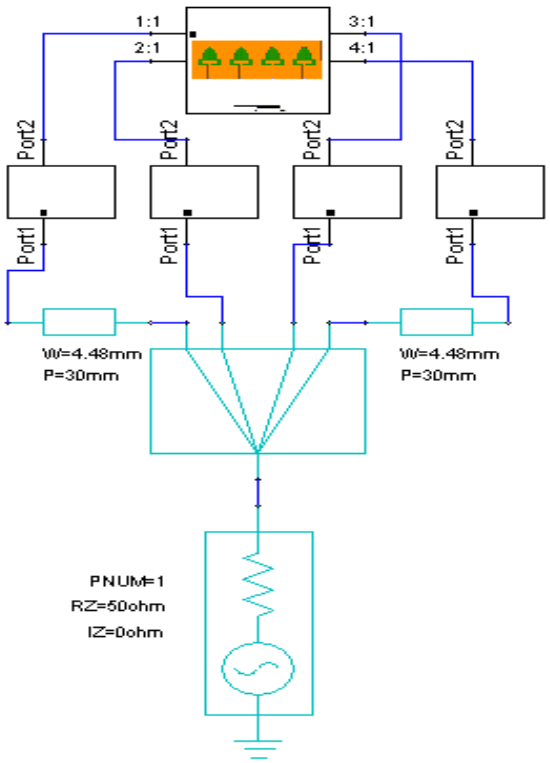

Figure 5.14 Pushing the excitations into HFSS through Dynamic Link.

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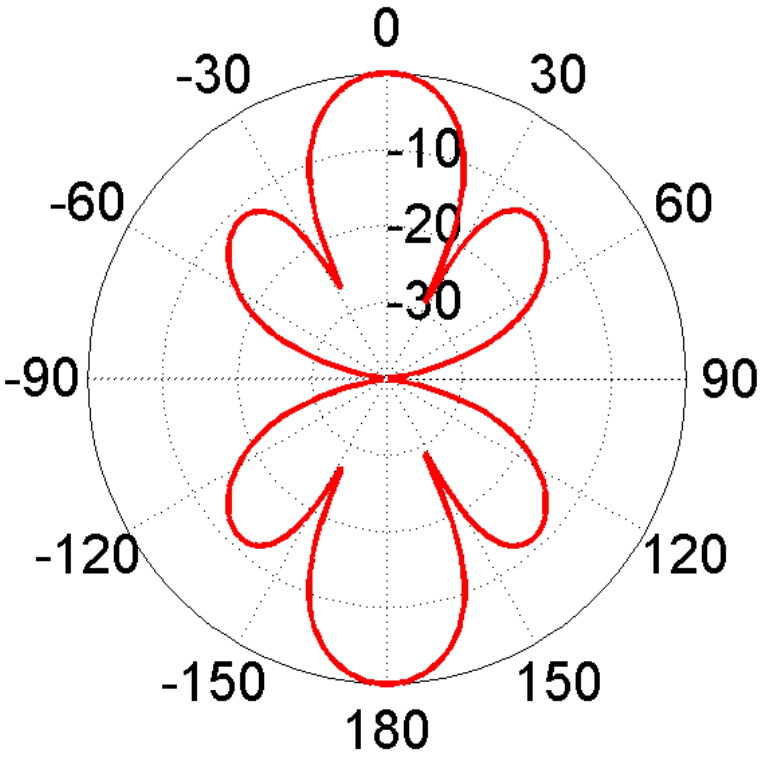

Figure 5.15 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=0 degree. Peak gain=9.6 dBi.

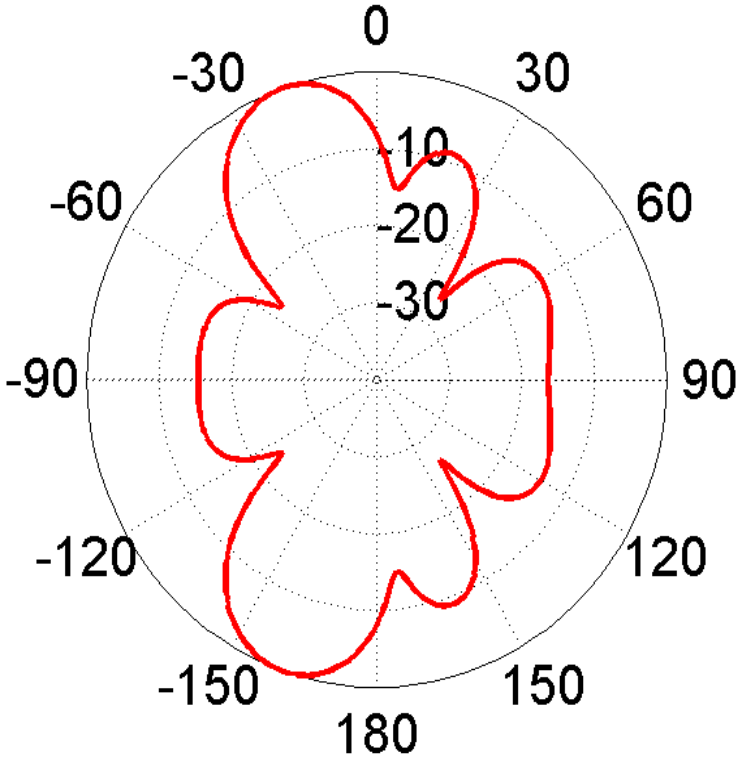

Figure 5.16 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=-20 degree. Peak gain=8.8 dBi.

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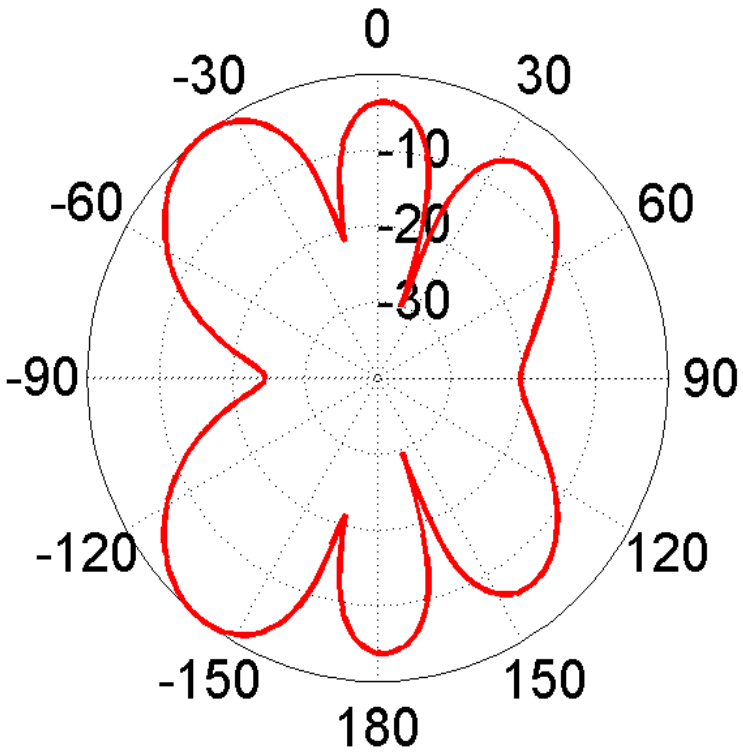

Figure 5.17 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=-35 degree. Peak gain=5.7 dBi.

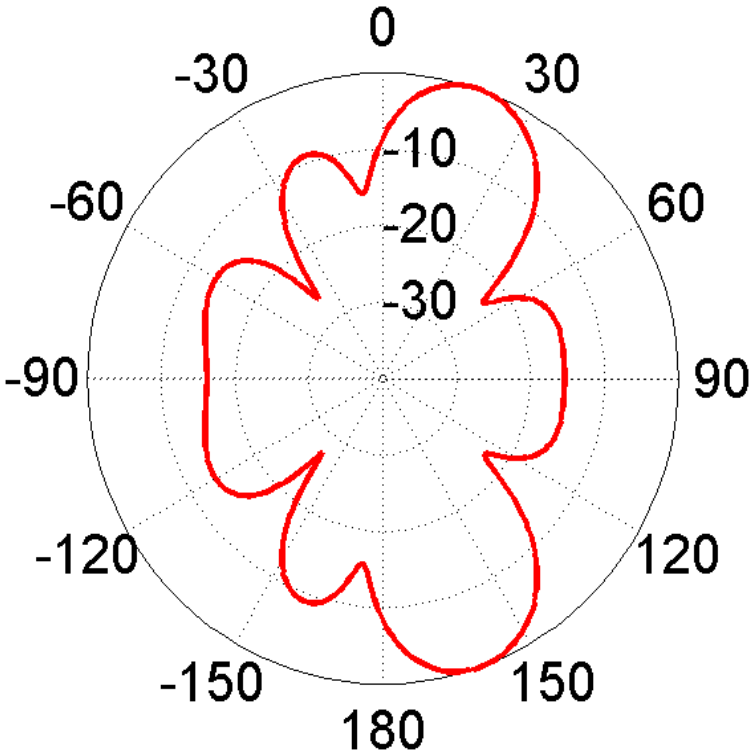

Figure 5.18 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=20 degree. Peak gain=8.8 dBi.

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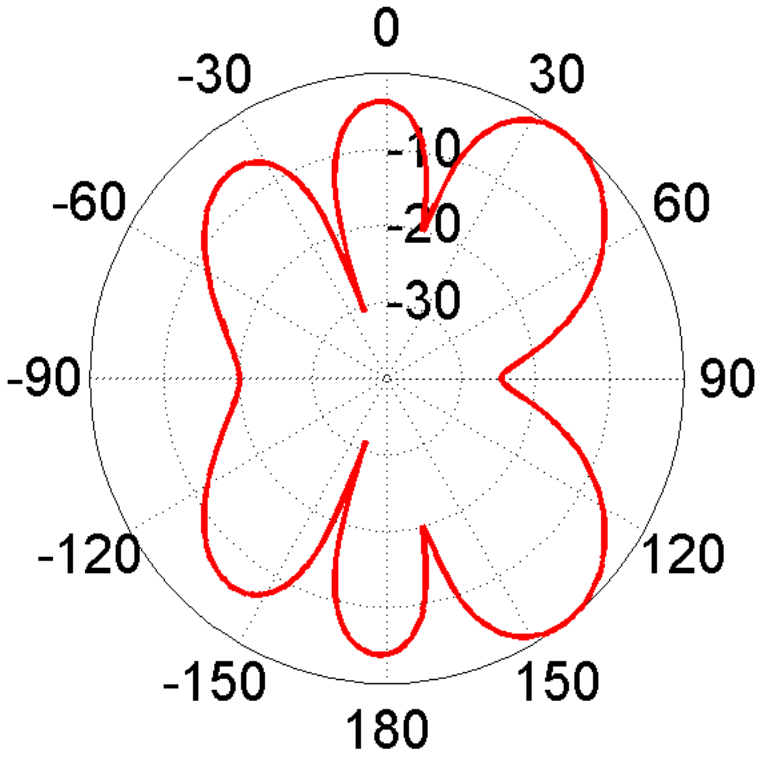

Figure 5.19 Radiation pattern of the slot array with the beam peak directed along $\boldsymbol{\theta_0}$=35 degree. Peak gain=5.7 dBi.

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CONCLUSION

First a four-element linear microstrip patch phased array antenna system is studied and designed. By designing, fabricating and measuring the insertion loss and delay characteristics of delay lines consisting of GaAs SPDT switches and DC blocking capacitors.

It is shown that the array beam can be scanned in desired angles 35˚, 20˚, 0˚, -20˚ and -35˚. The effects of the switch losses and the phase delays were taken into consideration by performing circuit plus antenna co-simulations in Ansys Designer.

Second, the fabricated and measured delay line characteristics were incorporated once again with a broadband coplanar waveguide fed slot antenna and wideband beam scanning is demonstrated at various scanning angles.

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FUTURE WORKS

In this research we observed that we could scan the beam of an array by changing the progressive phase shift β. The arrays we modeled have been simulated using HFSS and Ansys Designer but not fabricated.

The fabrication of the microstrip patch array and the semicircular slot array would allow understanding of the practical behavior of the array in the real world.

Similarly, other less loss switching systems such as MEMs could be studied. High power switches as GaN switches can be studied as well. Finally, a specific application can be considered and a wideband high gain planar phased array can be developed.

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